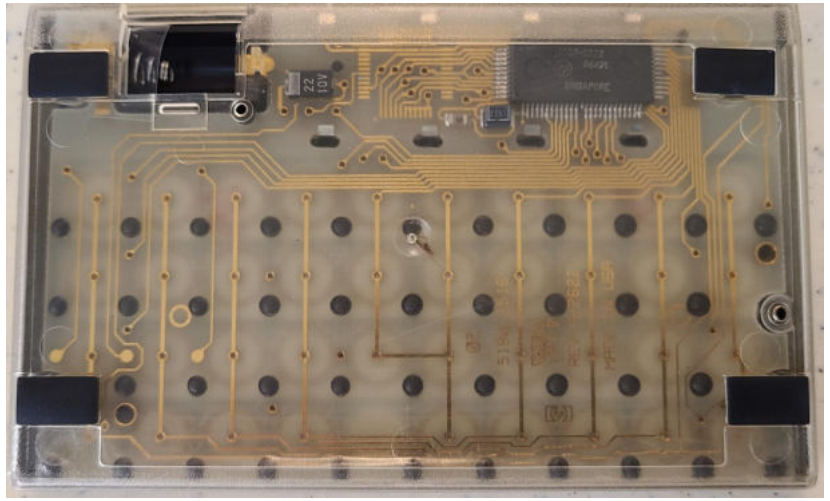
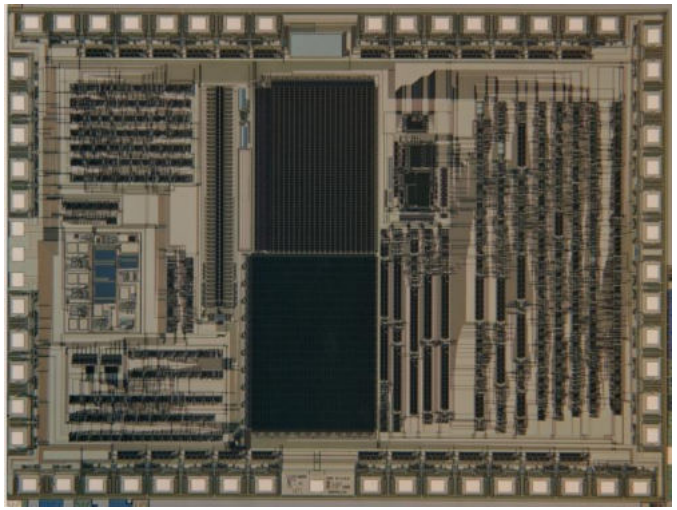
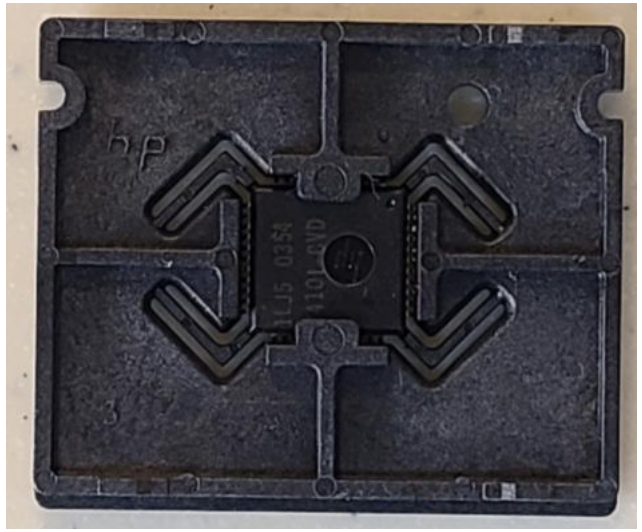
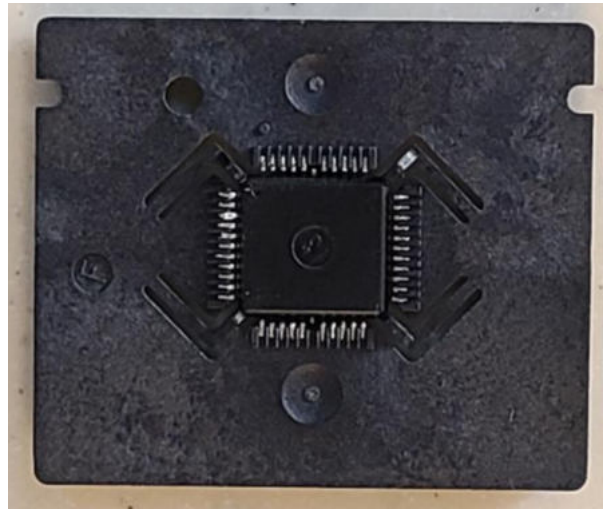




Single Chip Series Ten (SST)

Chuck McCord

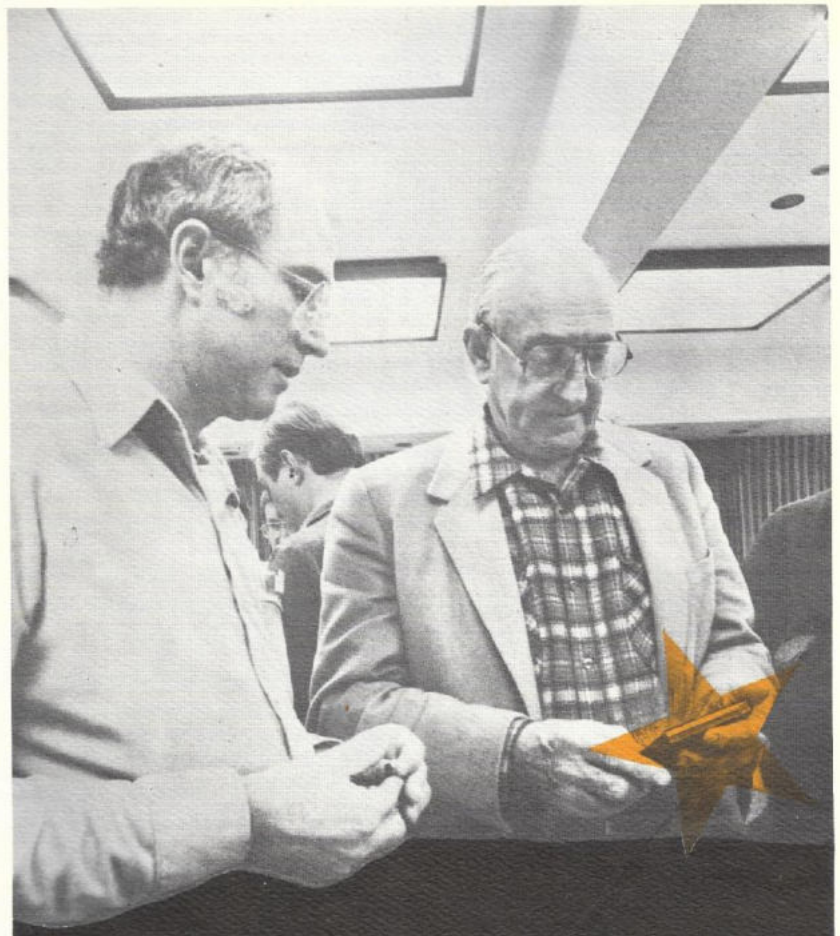




Outline

- **Voyager Context/Challenges**
- **What is SST**
  - **Project goals**
  - **HP organization context**
    - **Corvallis Site**
      - **ICBD History**
      - **Why Corvallis**
      - **Calculators, Portable Computers, Components**
    - **Return of the Jedi**
  - **IC**
    - **Design team**
    - **Design description**
    - **Design Process**
    - **Verification**
  - **Project surprises**
  - **Summary**
  - **Epilogue –then & now**
    - **Post SST: HP12C,DM12L**
    - **Semiconductors**
    - **HP Site**

October 1981
CALCULETTER
For Employees of the Corvallis Division



The star of the show, the HP 11-C.

Dick Moore introduces Dave Packard, co-founder, to Corvallis' newest product.

It Happened!

By Rebecca Perry

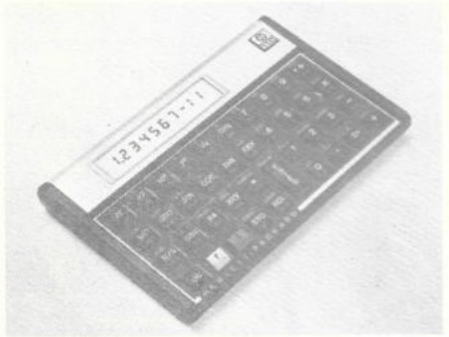
"Count-down!" It means waiting; hoping; feeling nervous and excited. It means something BIG is about to happen.

And something big *did* happen with the official lift-off of the HP-11C and HP-12C on September 16, 1981.

The introduction of the new "Voyager" family comes a few months before the ten-year anniversary of the world's first scientific hand-held calculator introduced by HP in 1972; and it marks a new dimension in both scientific and financial calculators.

The HP-11C scientific and HP-12C financial calculators *look* different; they are ½ inch thick, slim enough to slip into a pocket, and weigh only four ounces. But they are definitely not fragile. Exceptionally tough quality assurance tests have been imposed to ensure their ruggedness and reliability.

The models have many features in common, including a liquid-crystal display; CMOS(complementary metal-oxide-semiconductor) circuitry; continuous memory; a horizontal keyboard design; and several general and statistical analysis functions. Low-level power consumption makes it possible for the calculators to use disposable button-cell batteries, which cost about $1 a piece and are replaced about once a year.



The two calculators have distinct characteristics that aim their application toward specific professional areas.

The HP-11C Slim-Line Programmable Scientific Calculator is capable of solving complex scientific and engineering problems with features such as:

- 15 program labels
- Indirect addressing
- Conditional tests
- Flags
- Four levels of nested subroutines
- 200 line memory
- Program review with scrolling
- Insert and delete editing
- Conditional and unconditional branching
- Controlled looping
- User mode.

The *HP-12C "Slim Line" Financial Calculator* is capable of solving tough business calculations with its many powerful functions, including:

- Compound interest solutions
- Amortization
- Discounted cash flow analysis with net present value and internal rate of return
- Bonds and annuities calculations
- Three types of depreciation schedules
- A unique amortization function that calculates odd days' interest accruals
- Calendar function.

Highlights of Voyager's introduction to the world included coverage by TV channels 9 and 13 in Eugene, a front-page story in *Electronics Engineering Times*, and prominent coverage in *Electronics* and other trade magazines.

40th Anniversary
HPCC
22, 23 Oct 2022

From Corvallis Components Operation General Manager

Launching Voyager

The Voyager project which culminated in the recent introduction of the HP-11C and the HP-12C calculators presented two major challenges for the Corvallis Components Operation.

The first was in packaging of the integrated circuits. Not only was the necessary pin count for these IC's high (up to 72 leads) but the space available in the "thin line" package of the calculators was too small to accommodate the height of our normal dual-inline package - familiar "DIP". The solution was the "quad pack", with leads on all four sides of the package (versus two on the DIP) and a low profile molded body to meet the space requirements. A team of engineers from the calculator lab and Components developed the package and the necessary tooling. Included was all new molding, lead forming and package handling equipment, plus of course, new lead frames and a large amount of detail "debugging" of the tools and parts. The resulting set of tooling is now in place and is running in our Singapore components production line. Refinement and fine-tuning of this new packaging system is continuing and we expect it will be our main IC encapsulation method for the next several years.

The second big challenge presented to Components by the Voyager effort involved our MOS Fabrication area. To bridge the time gap between availability of a circuit from an outside vendor and the calculator production start-up, we fabricated the largest CMOS chip yet done in our shop - 6.53 by 6.42 mm (or 0.257 by 0.253 inches for those of you not yet metricized!). Even though this is too big for large scale production in our present CMOS process, we built tens of thousands of these circuits and made introduction of the new calculators possible months earlier than would otherwise have been the case. Our new, higher density MOS process will be starting up early next year and will make our in-house capability cost effective for these large, complex circuits.

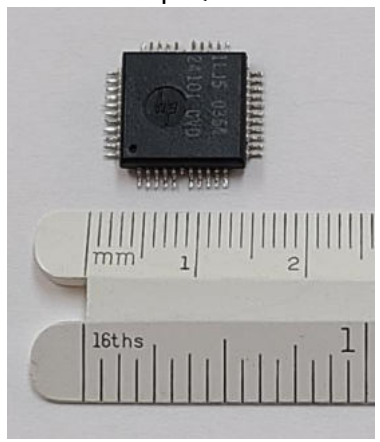
These packaging and chip fabrication efforts are typical of the specially developed processes and parts in Corvallis Components Operation - all aimed at making better end products for our calculator and computer customers. All of the people involved (I counted 20 and decided not to list them all!) can be justly proud of their contribution to Voyager.

Ed Shideler
Corvallis Components Operation
General Manager

Voyager's two major challenges for the Corvallis Components Operation

High pinout Quad Flat Pak (QFP) package

44p QFP



Voyager required the largest CMOS chip yet done in our shop … "*even though this is too big for large scale production* in our present CMOS process, we built tens of thousands of these circuits and made introduction of the new calculators possible months earlier…"

"Our new, higher density MOS process will be starting up early next year and will make our in-house capability cost effective"

SST Project Goals

- Voyager doing well
- Voyager was high volume (for HP)
- Wanted to cost reduce Voyager
  - Reduce number of ICs from 2 to 1 for HP10, HP11, HP12, HP16 and
  - Reduce number of ICs from 3 to 2 for HP15
  - Use a 2 layer PCB
- SST viewed as a *short term* cost reduction as Voyager would be replaced by Pioneer with 1-2 years

ICBD History – 1977 thru 1984

	1977	1978	1979	1980	1981	1982	1983	1984
Top Grossing Movie	Star Wars	Grease	Kramer vs. Kramer	The Empire Strikes Back	Raiders of the Lost Ark	E.T.	Return of the Jedi	Beverly Hills Cop
#1 Song	Tonight's The Night– Rod Stewart	Shadow Dancing– Andy Gibb	My Sharona– Knack	Call Me –Blondie	Bette Davis Eyes– Kim Carnes	Physical– Olivia Newton John	Every Breath You Take –The Police	When Doves Cry– Prince

CMOSV (6 microns)
NMOSV

CMOSC (4 microns)

CMOSG (3.5 microns)

Milestones

1975 – Corvallis Site opened

HP Advanced Products Division outfits Facility 1 in B3 for calculator IC Mnfg.

Dave Packard visits site for division review

1st HP–Corvallis Summer Picnic held at Silver Creek Falls

3" product wafers started in B3 Fab

NMOS & CMOS product lines merge

New wafer mnfg process developed for each new product

Wafer boxes introduced to B3 fab just before:

Corvallis site splits into 3 divisions: ICs, calculators, and desktop computers

SAMM comes online

Mt. St. Helens erupts Fab concerned about ash clogging air filters.

4" product wafers started in B3 Facility 3

B3 air shower built

Products designed to be mnfg using standard proces: (much less tweeking)

1st Spring Fling celebration

CCO becomes Northwest Integrated Circuit Division (NID)

Bunny suits bought for B3 Fab (previously smocks, gloves, snood, and shoe covers)

CVD PCD CCO ICBD

Why Corvallis?
Corvallis CMOS Fab

HP Organizations

From my vantage point

CCO becomes NID (1984)

SST

CVD | PCD | CCO

1980

CTG created from:

- ICBD/NID- NW IC Division
- FID- Ft Collins IC Division
- CID- Cupertino IC Division

ICBD created(1990)

- BU doing ICs for many HP Divisions

t

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SST

Behind schedule before it started

Program manager: “Lord Vader, this is an unexpected pleasure! We are honored by your presence.”

Vader: “You may dispense with the pleasantries commander. *I am here to put you back on schedule*!”

PM: “I assure you Lord Vader, my men are working as fast as they can.”

Vader: “Perhaps I can find *new ways to motivate them*.”

PM: “I tell you, this station will be operational as planned.”

Vader: “The emperor does not share your *optimistic appraisal of the situation*.”

PM: “But he asks the impossible! I need more men.”

Vader: “Then perhaps you can tell him when he arrives.”

PM: “The emperor is coming here?”

Vader: “That is correct, commander… And he is most displeased with your *apparent lack of progress*.”

PM: “We shall double our efforts!”

Vader: “I hope so commander, for your sake. The emperor is not as forgiving as I am.”

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SST's International Design team

- Corvallis team- couldn't have asked for better…

  very strong EEs with calculator system backgrounds
  - HP41 CPU designer
  - Voyager IC designers

- Matt Borg
- Allen Brown
- Ray Davis
- Don Reid
- Eric Gullerude
- Chuck McCord

- Singapore team- extended FSEs in Corvallis
  - Awesome group of BS, MS EEs that went on to be
    - HP/Agilent Penang site R&D Manager
    - HP Singapore site R&D Manager
    - Engineers, Directors & VPs at HP and other companies

- Frederick Cheong
- Pan Kok-Chin
- Pang Chong
- *

- We worked long hard hours. We had a blast. We formed friendships that lasted decades.

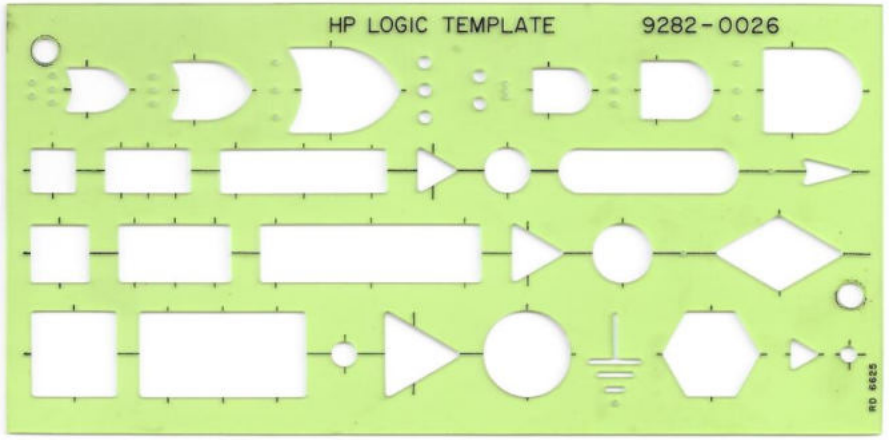
* Profuse apologies to any left out… it wasn't intentional. These are those that I and the 3 team members I contacted could remember from 40 years ago.

SST's Design

- Voyager schematic hand drawn on 1 E-size blueline (key tool used is pictured)

- All previous designs were full chip custom layout
  - There was a fair amount of skepticism that standard cells could achieve cost effective densities for high volume calculator designs (i.e., were CAD tools capable of achieving cost effective densities in current CMOS processes).

- The SST design was partitioned into custom blocks and standard cells
  - Used custom cells for density: RAMs, ROMs, Shift registers, PLAs, Analog
  - Entered schematic for Standard Cells.

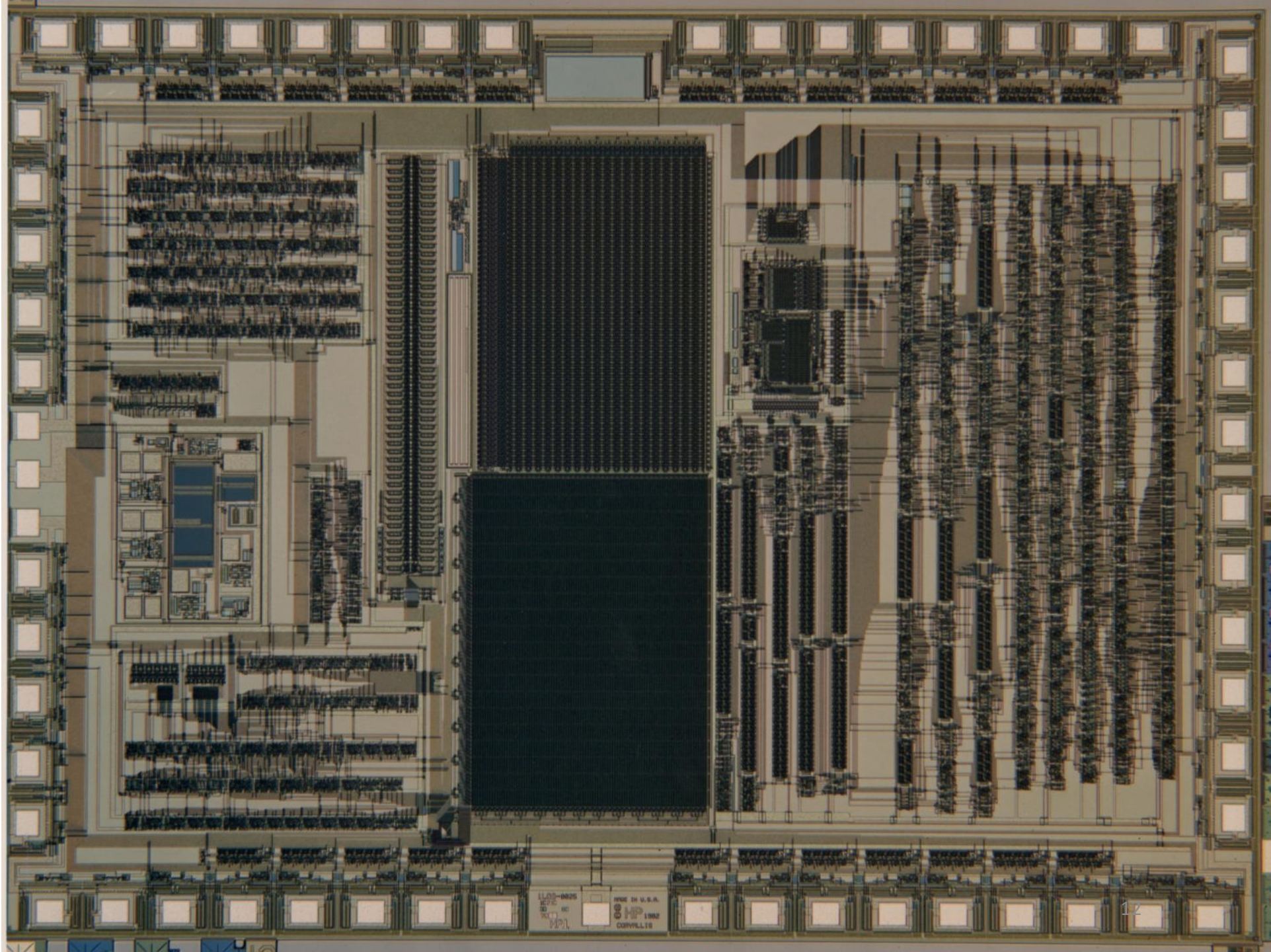


SST

(Single Chip Series 10) Design Description

Single Superchip for
HP10,11,12,16
HP15 2 chip implementation

First HP standard cell CMOS calculator IC

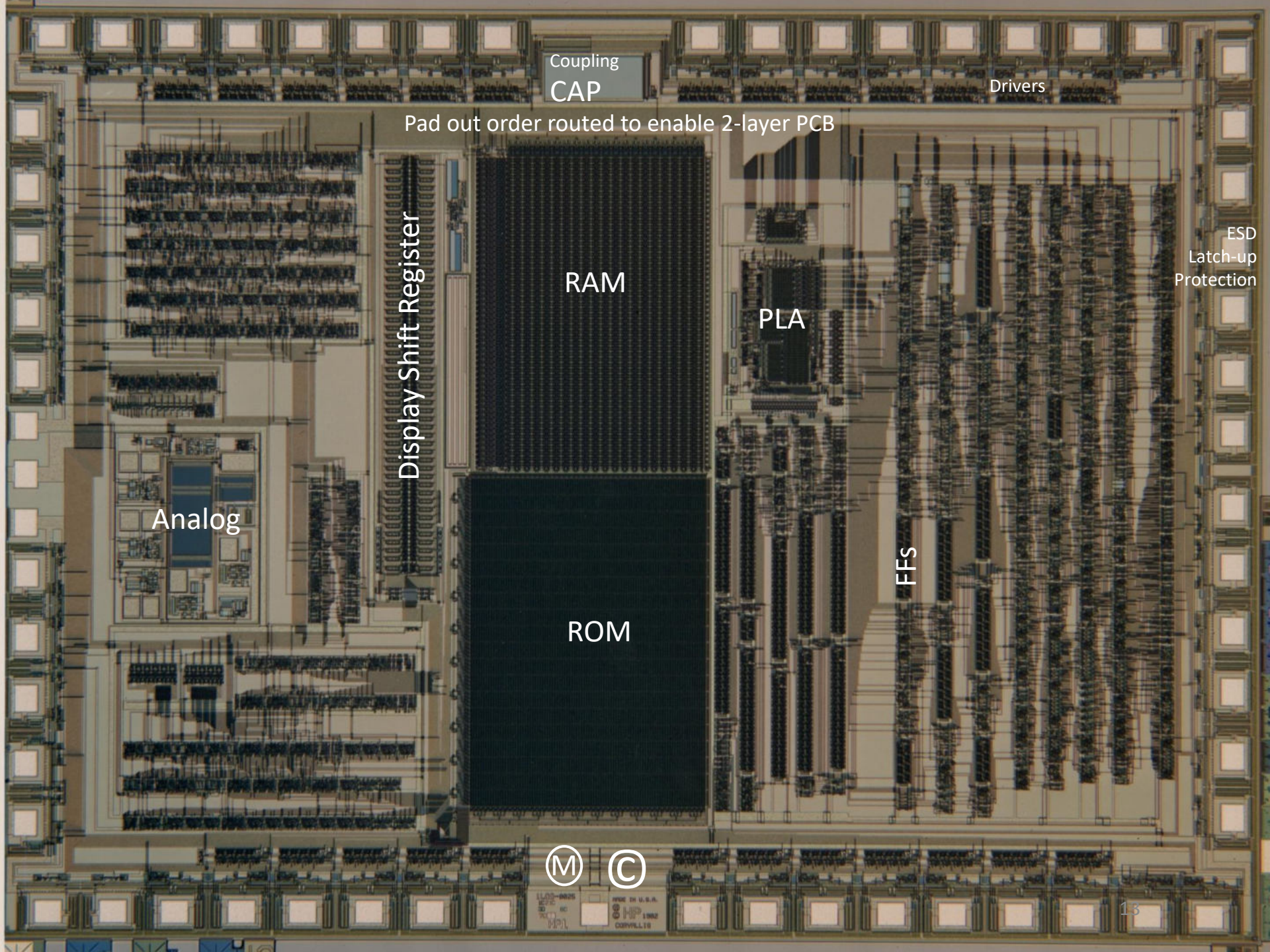


SST

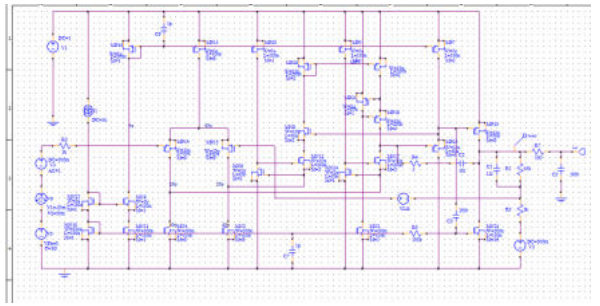
(Single Chip Series 10)
Design Description

CPU
- PLA
- Standard Cells
- Registers

RAM
ROM
LCD Display Driver
Keyboard Interface
Clock generation



Verification



During design:

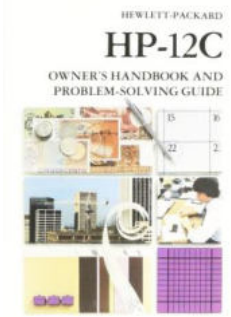
Simulation-Used Voyager *functional* test vectors to logic simulate full chip
Voyager – very high quality low PPM
HP SPICE simulated custom cells, critical timing paths
SCOPE – Sandia Controllability and Observability program used to evaluate testability
DRC, LVS- run on Amdahl in Loveland, Colorado

During manufacture:

ATE- Schlumberger Sentry 7, Sentinel testing- full pattern, electrical spec testing
Did multipattern RAM retention testing
ROM verification

Prototyping:

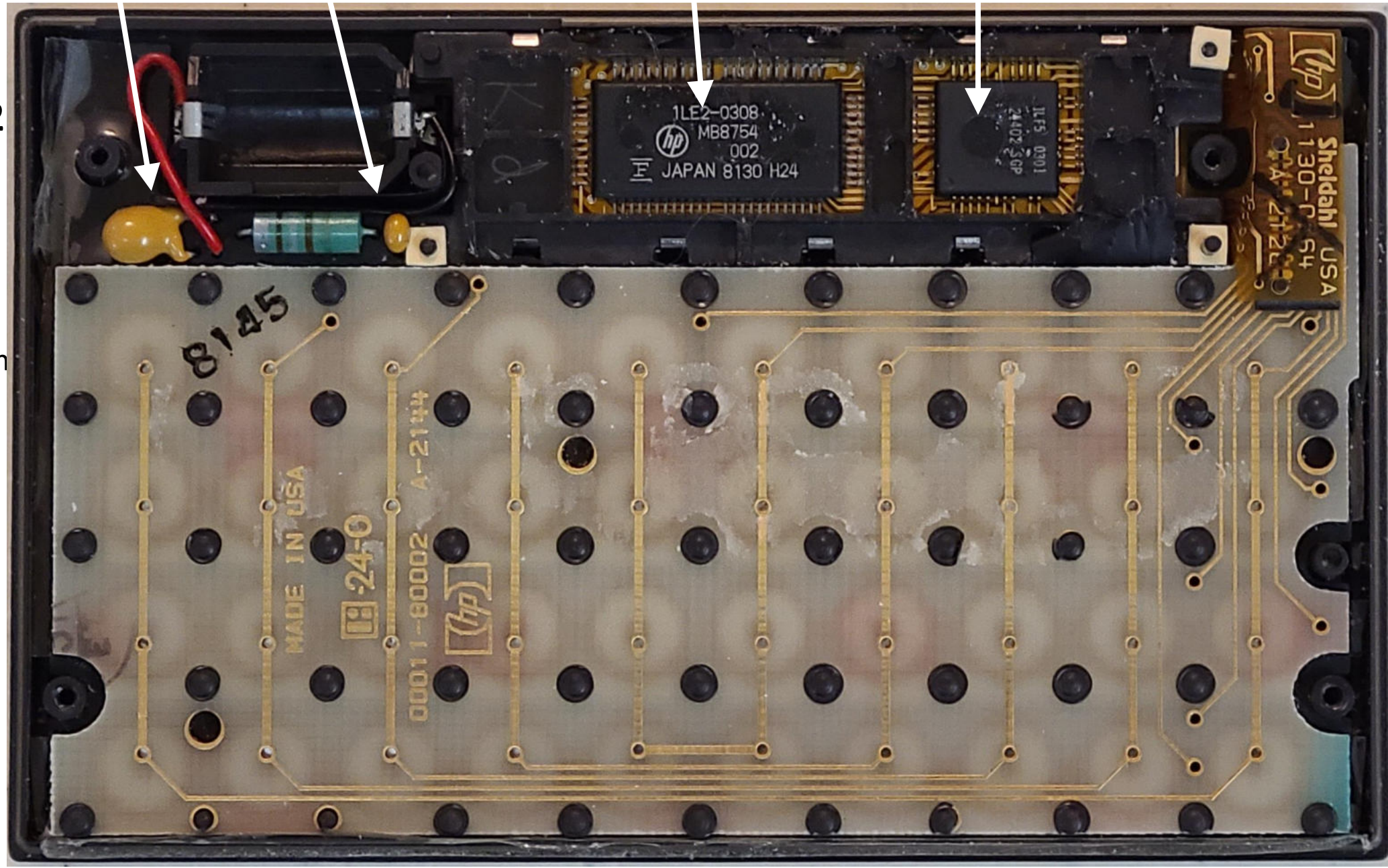
Did ***large proto builds*** (had people on site run units thru paces)
Also had technicians ***verify every user manual example*** for all models



Voyager System
HP10, HP11,HP12

- (2) ICs
- (2) PCBs
  - 1 Higher cost
- Plastic Dam
- PCB-PCB connection
- Wires
- Non-surface mount R and Cs

* Big **THANK YOU** to Bob Prosperi for this photo!



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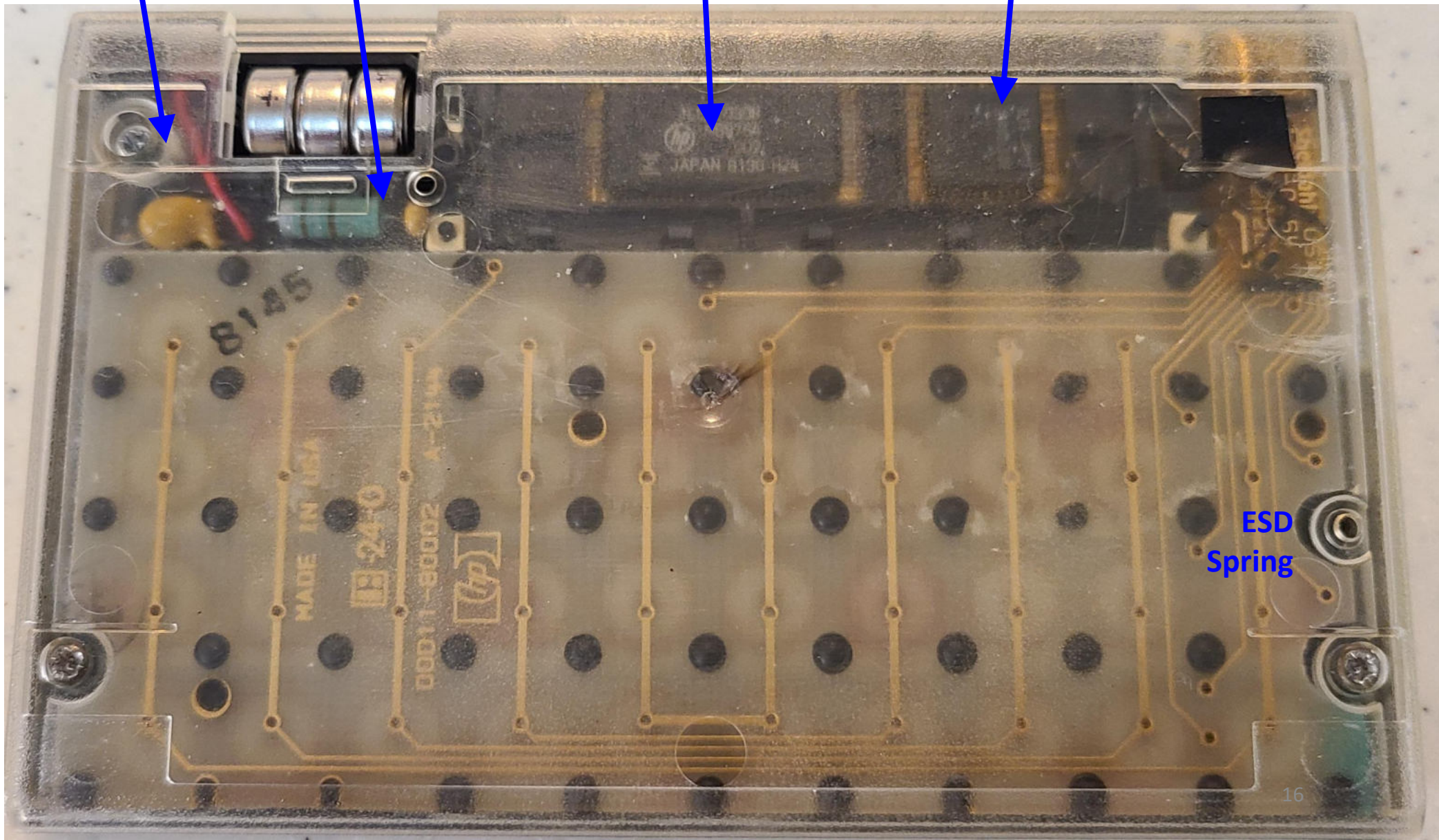
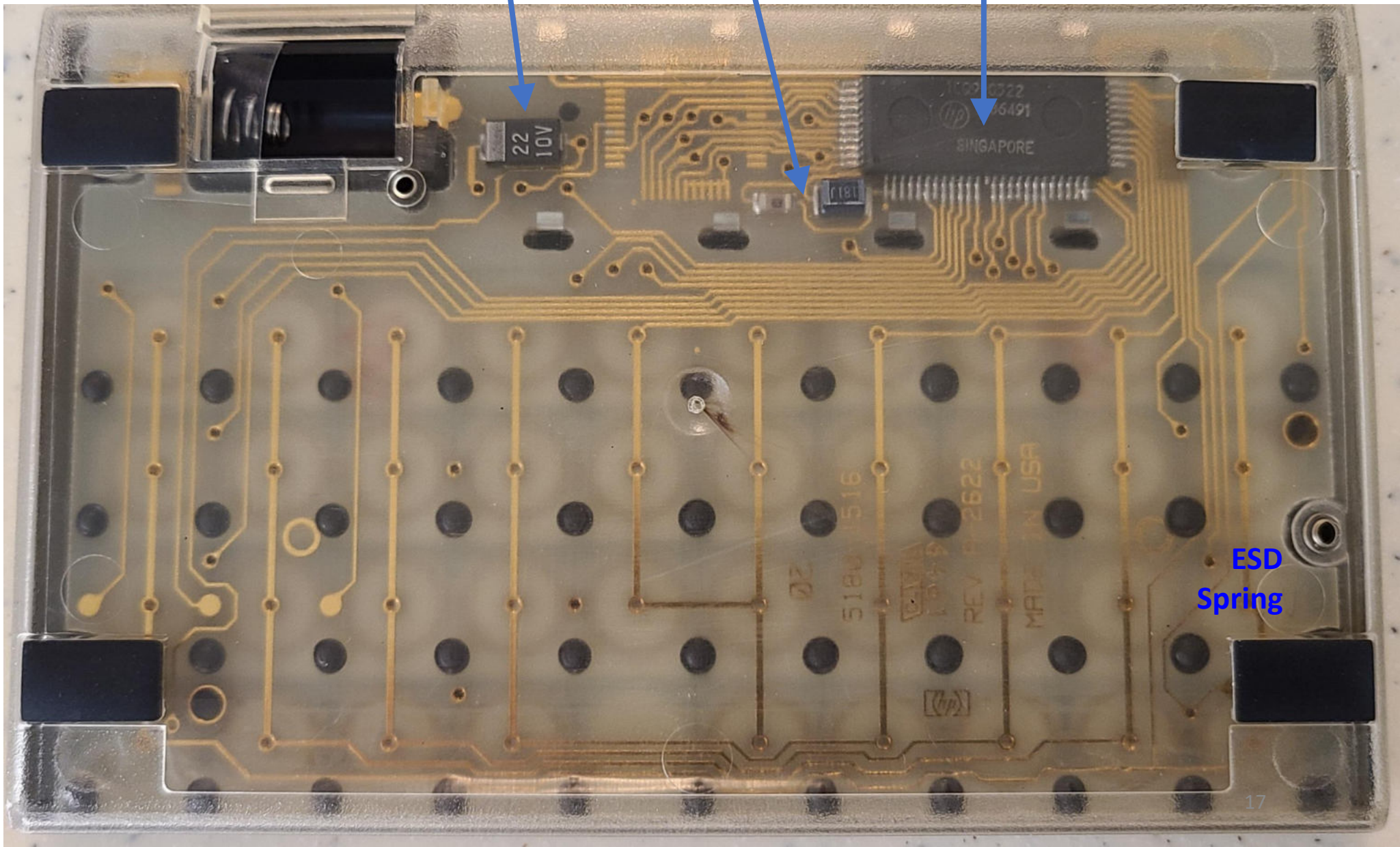


SST Voyager System

HP10, HP11, HP12

- (1) IC
- (1) 2 layer PCB
- No Plastic Dam
- No PCB-PCB connection
- No Wires
- All surface mount R and Cs



Project Surprises

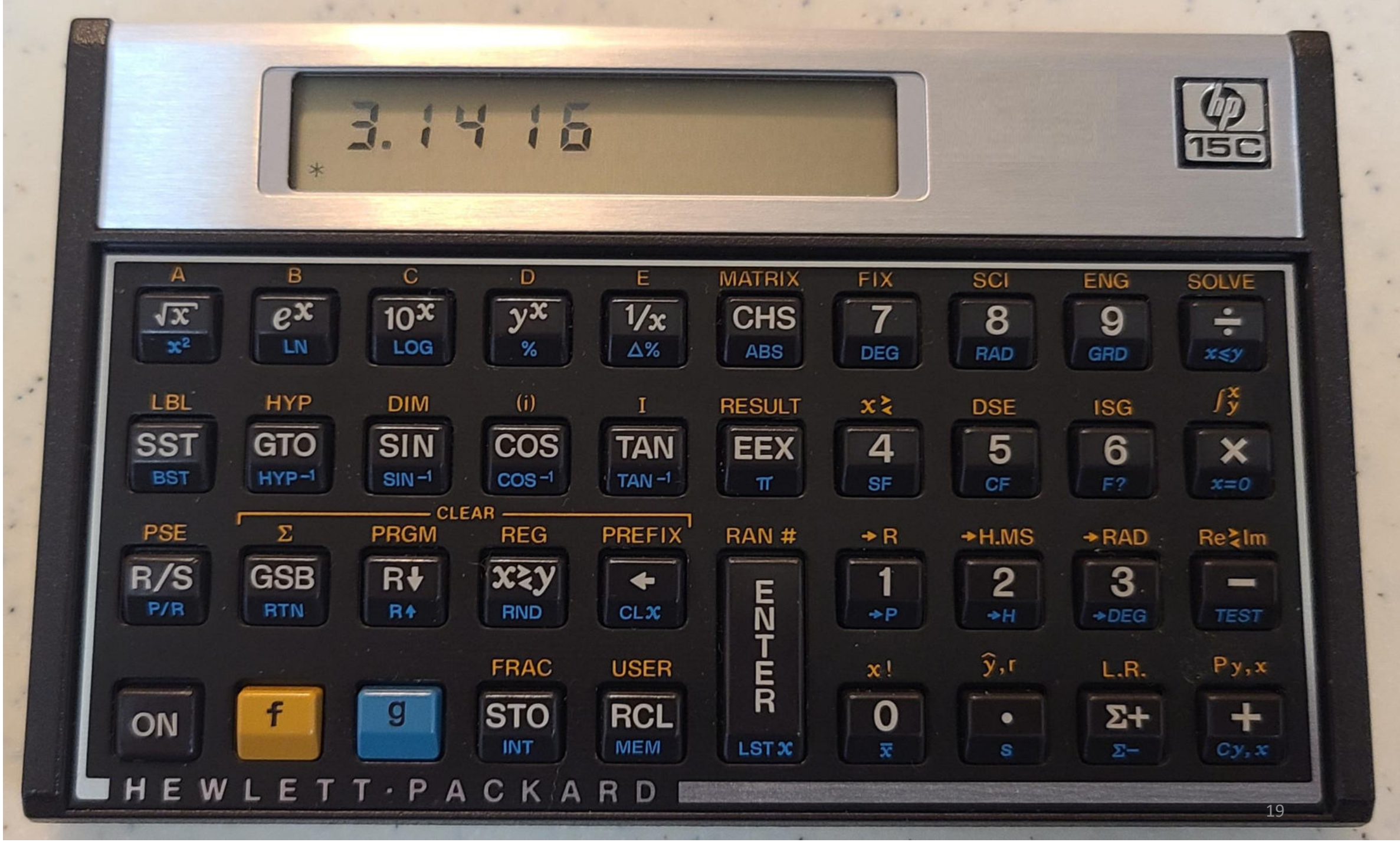
- **Big one-** HP12 was not obsoleted by Pioneer & is still going strong.
  The SST project had a very positive ROI.
  The HP12 outlasted its fab process.
  SST was not the last Voyager reimplementation.

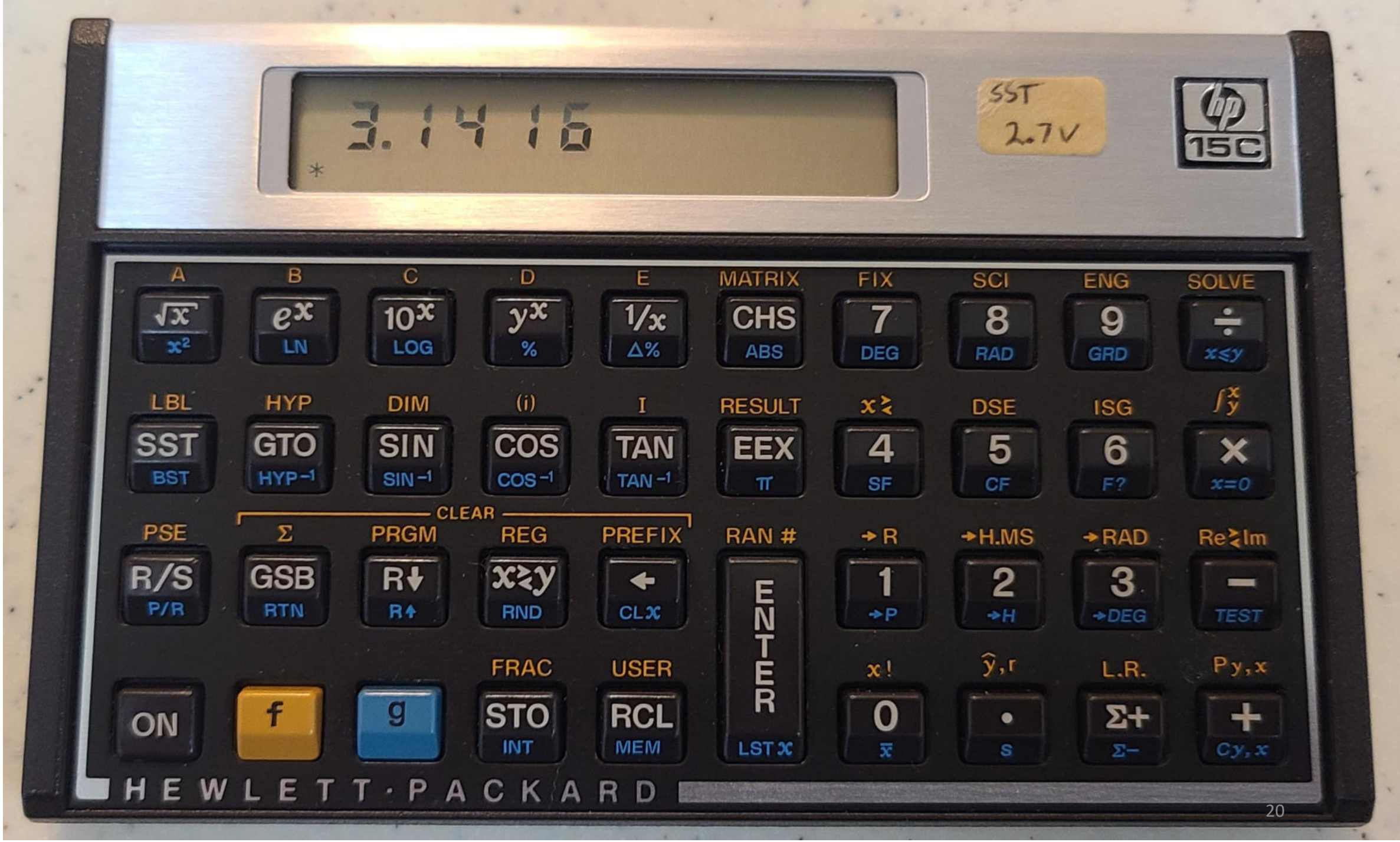
SST

- How much less robust semi-custom auto place and routed designs were than their original custom designs.
  - When all appropriate parasitic were considered HP Spice was reliably spot-on accurate. Simplifying assumptions led to missed timing races and voltage dependent behaviors.

One example found late in development was the ON-. Timing race.

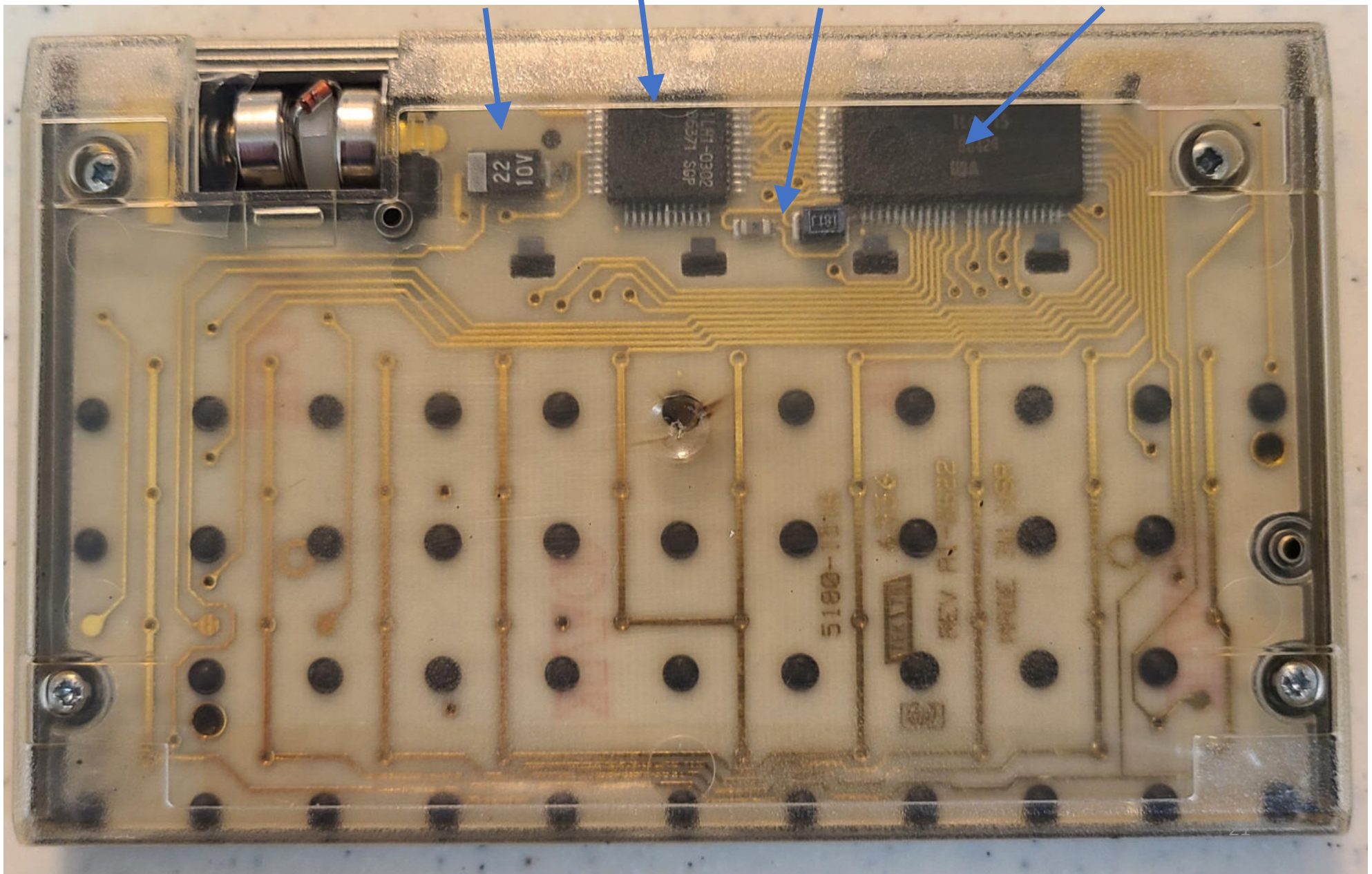
3,1,4,1,5,9,2,6,5,4,


3.1416
hp 15C
A B C D E MATRIX FIX SCI ENG SOLVE
√x x² | eˣ LN | 10ˣ LOG | yˣ % | 1/x Δ% | CHS ABS | 7 DEG | 8 RAD | 9 GRD | ÷ x≤y
LBL HYP DIM (i) I RESULT x≷ DSE ISG ∫ₓʸ
SST BST | GTO HYP⁻¹ | SIN SIN⁻¹ | COS COS⁻¹ | TAN TAN⁻¹ | EEX π | 4 SF | 5 CF | 6 F? | × x=0
CLEAR
PSE Σ PRGM REG PREFIX RAN # →R →H.MS →RAD Re≷Im
R/S P/R | GSB RTN | R↓ R↑ | x≷y RND | ← CLx | ENTER LST x | 1 →P | 2 →H | 3 →DEG | − TEST
FRAC USER x! ŷ,r L.R. Py,x
ON | f | g | STO INT | RCL MEM | 0 x̄ | • s | Σ+ Σ− | + Cy,x
HEWLETT·PACKARD

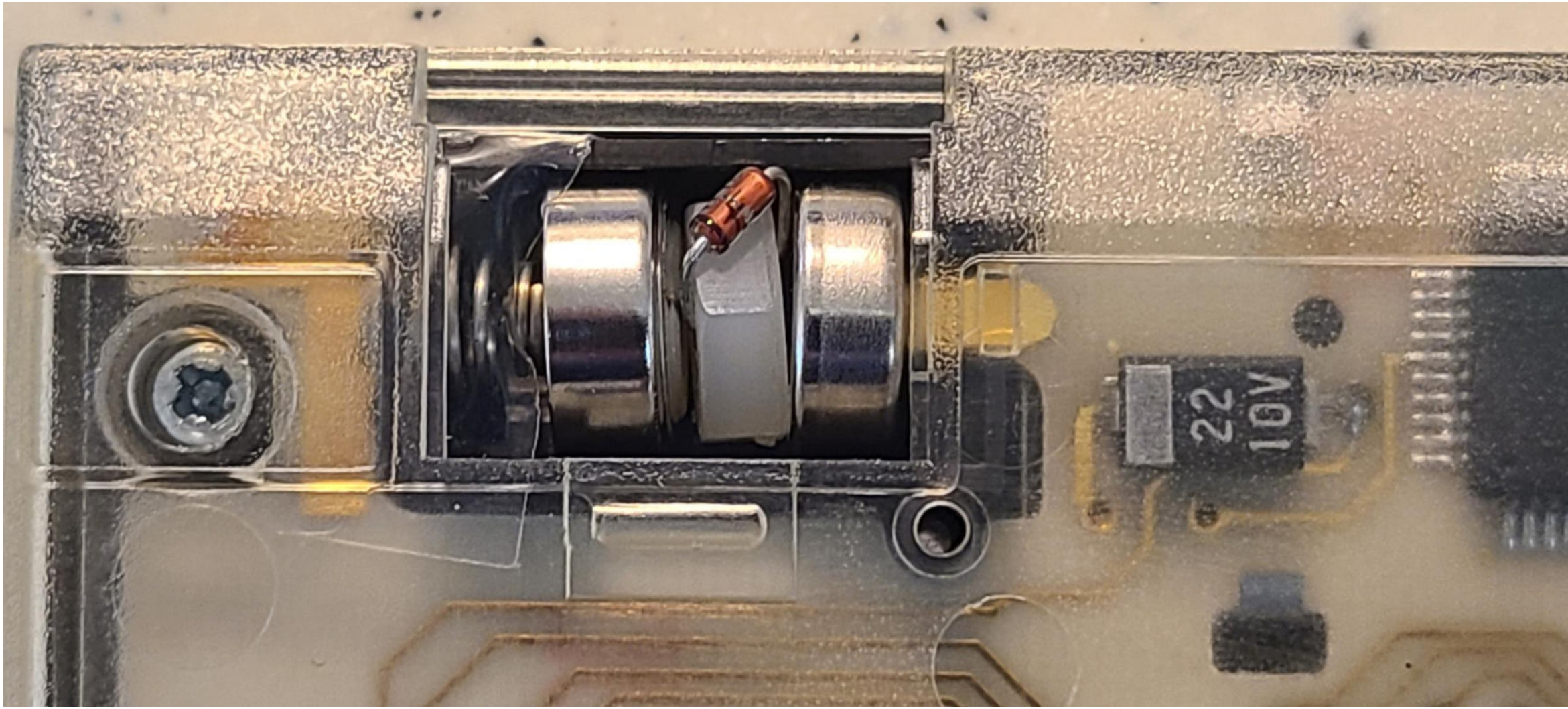

3.1416
SST
2.7V
15C
A B C D E MATRIX FIX SCI ENG SOLVE
√x x² | eˣ LN | 10ˣ LOG | yˣ % | 1/x Δ% | CHS ABS | 7 DEG | 8 RAD | 9 GRD | ÷ x≤y
LBL HYP DIM (i) I RESULT x≥ DSE ISG ∫yˣ
SST BST | GTO HYP⁻¹ | SIN SIN⁻¹ | COS COS⁻¹ | TAN TAN⁻¹ | EEX π | 4 SF | 5 CF | 6 F? | × x=0
CLEAR
PSE Σ PRGM REG PREFIX RAN # →R →H.MS →RAD Re≥Im
R/S P/R | GSB RTN | R↓ R↑ | x≥y RND | ← CLx | ENTER LSTx | 1 →P | 2 →H | 3 →DEG | − TEST
FRAC USER x! ŷ,r L.R. Py,x
ON | f | g | STO INT | RCL MEM | 0 x̄ | • s | Σ+ Σ− | + Cy,x
HEWLETT·PACKARD

Voyager System

HP15



Voyager System
Low Voltage Workaround



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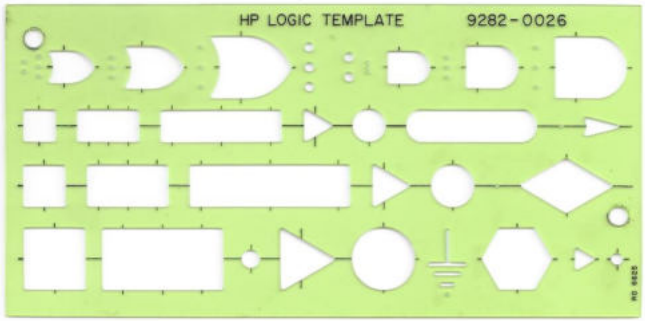
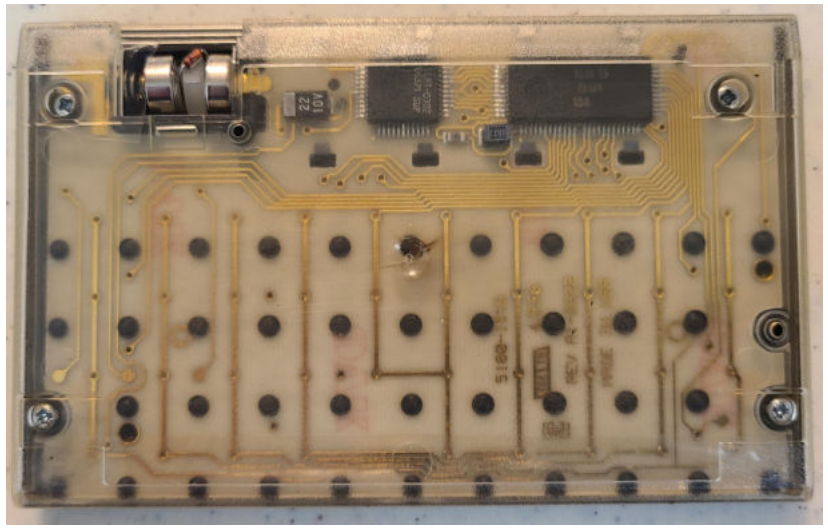
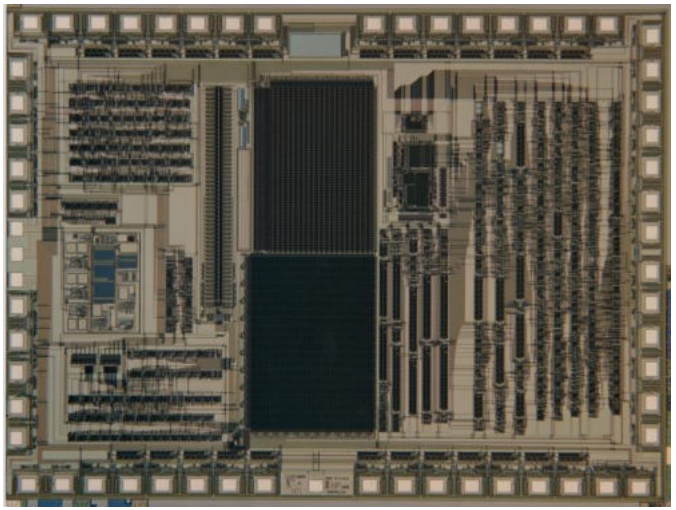


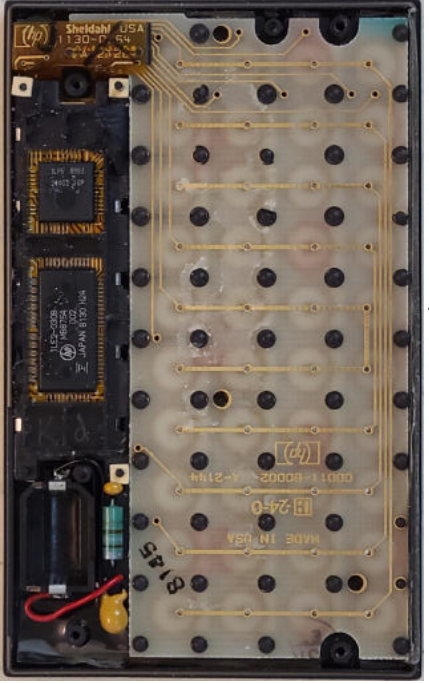




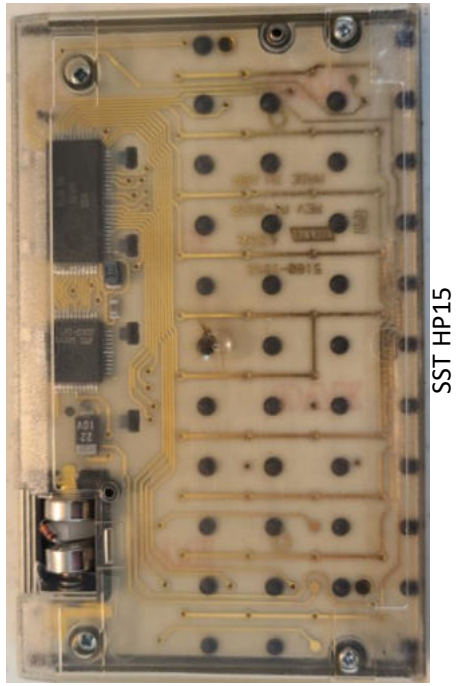
Thank You!!

3,1,4,1,5,9,2,6,5,4,

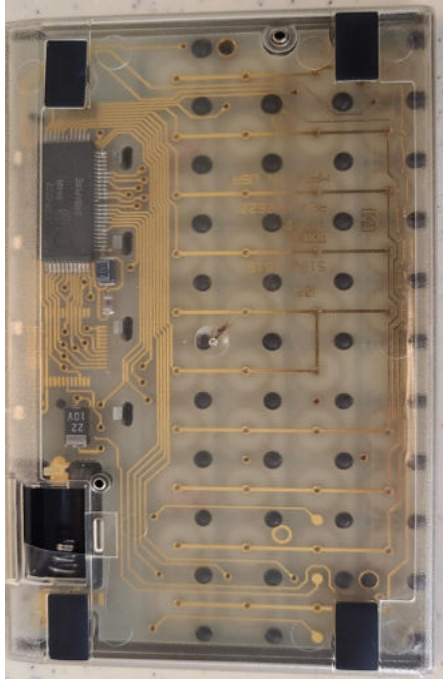
40th Anniversary HPCC 22, 23 Oct 2022



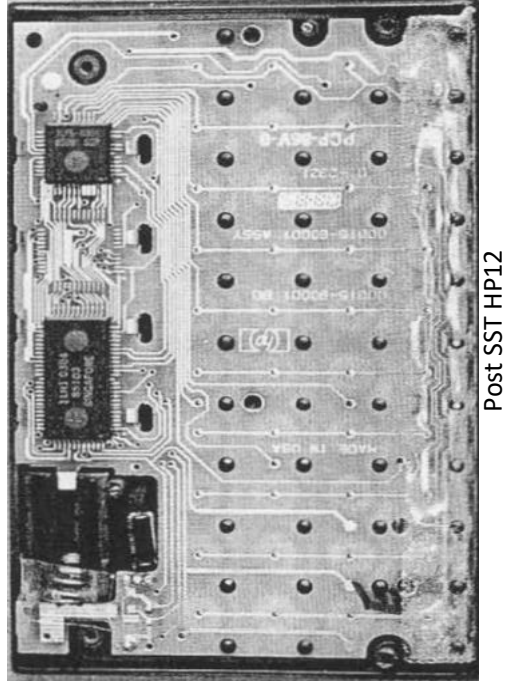
HP12C 1982wk18 USA 2218A04935



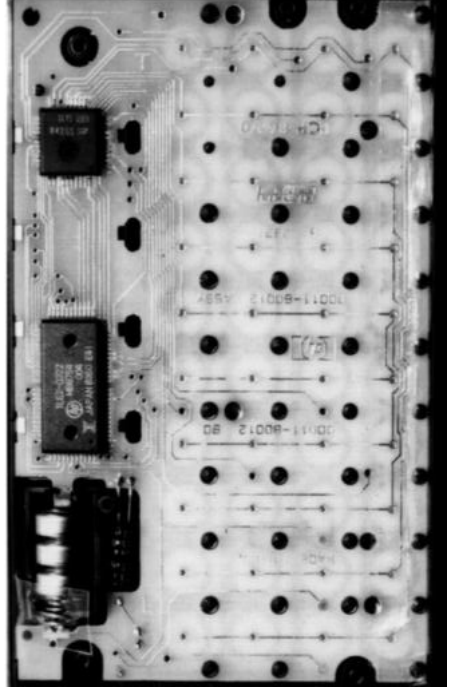
SST HP15



SST HP12 1982 USA 2222A#####

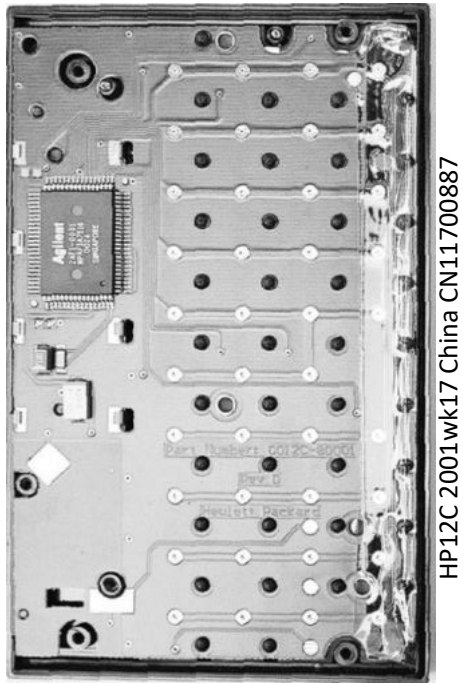


Post SST HP12



Post SST HP12

HP12C 1999wk29 Malaysia MY92902542



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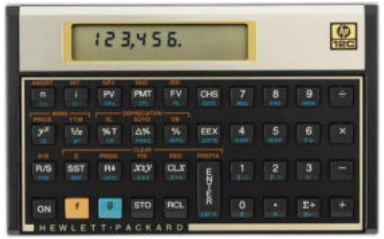

Voyager System

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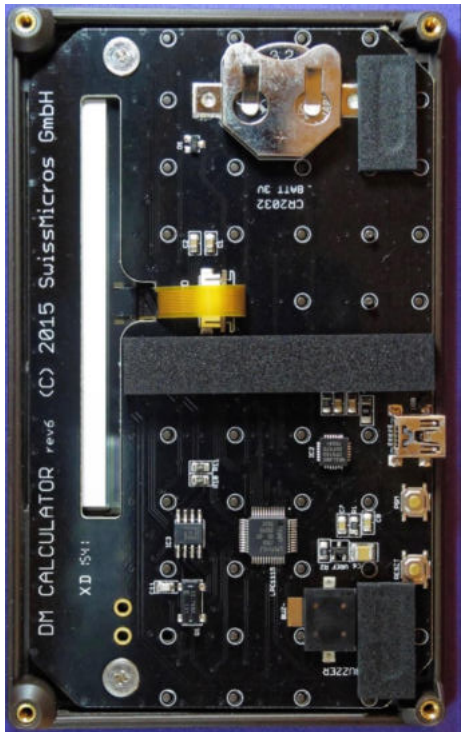
HP12C 2012 Invertec 4CY2320481



Swiss Micro DM15L

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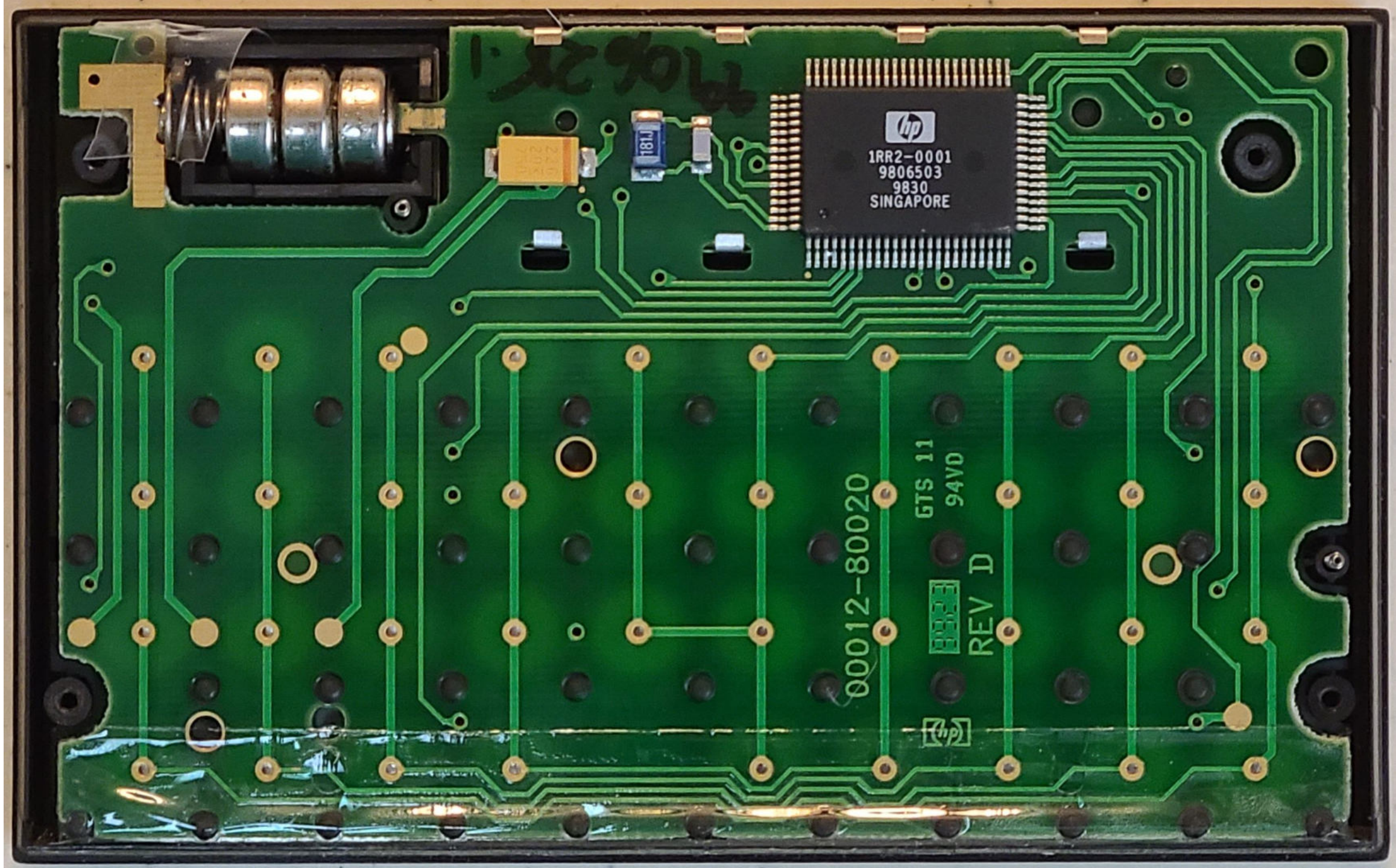

HP12C
1999wk29
Malaysia
MY92902542

MY92902542

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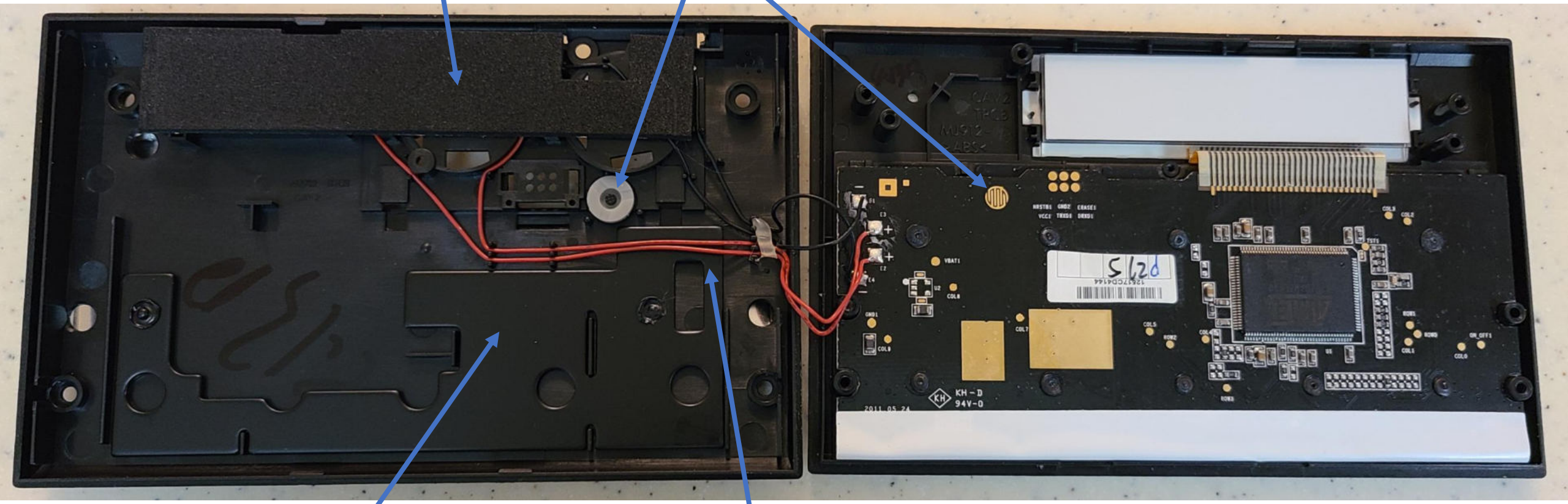
HP12C
2012 Invertec
4CY2320481

Foam LCD Support

Conductive Rubber Reset



Weight/ Back Stiffener

4 Battery Wires

* Big **THANK YOU** to Bob Prosperi for this calculator!

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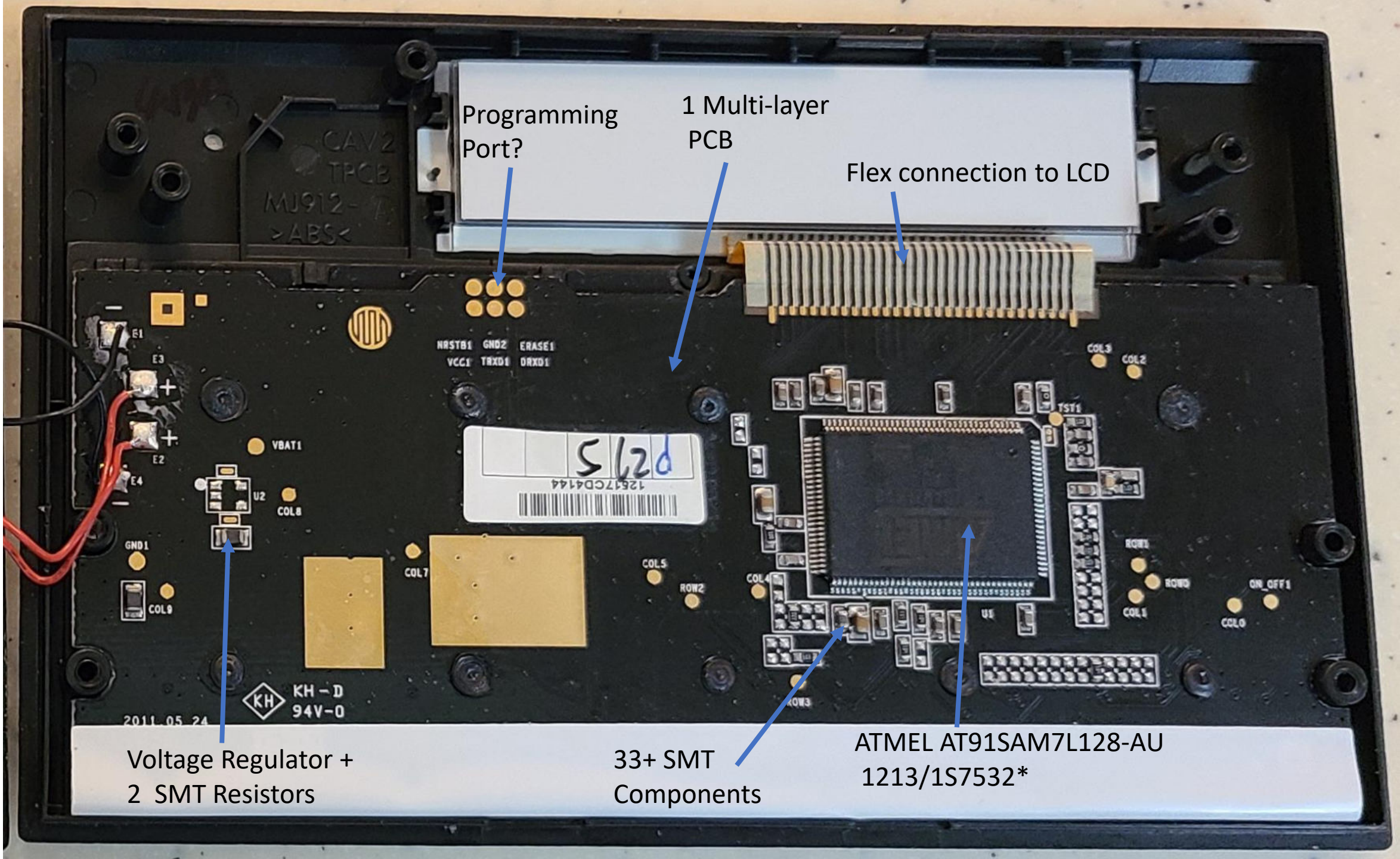
HP12C
2012 Invertec
4CY2320481

* ATMEL
128kb flash
6kb SRAM
7 Seg drv
USART
SPI
…



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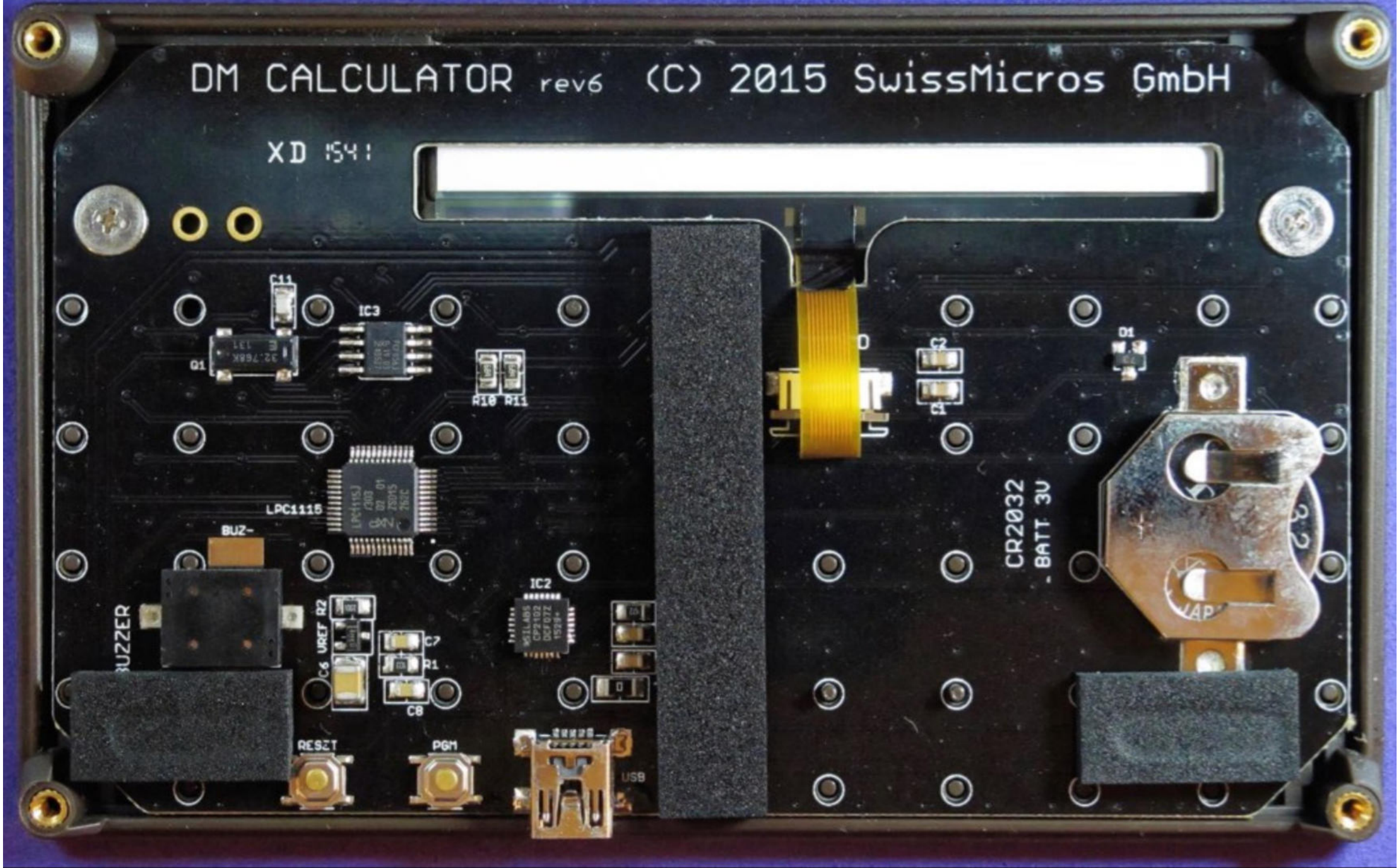
DM 15L



https://jepspectro.com/img/dm15/IMG_5283b.jpg

Epilogue- HP Semiconductors

- B3- fab for low leakage CMOS w/1 layer Poly, 1 layer Metal for calculators
- B2- higher volume, lower defect density CMOS fab for more advanced nodes for WW HP product use
- Offered foundry services (supercomputers, PC graphics chips, error correction, …)

- HP Transitioned Internal CMOS ICs → Foundry service customer
- Transitioned B2 Fab → Inkjet print head manufacturing

- Internal CAD → Industry CAD

HP CV Site over time

In **1980** only B3 & B4, w/B5 in progress

B3, B4, B5 are all standard HP Bigfoot buildings

- B4: Front lobby
  - Cafeteria
  - Offices
  - Plastic Molding, CNC machines
  - Wave solder
  - PCB & Final Assembly
- B3: CMOS fab, ATE, Offices
- B5: Initially empty (played Frisbee)

Later

- C: dedicated Cafeteria built as site grew
- B2: super bigfoot fab and office space
- Service had its own building

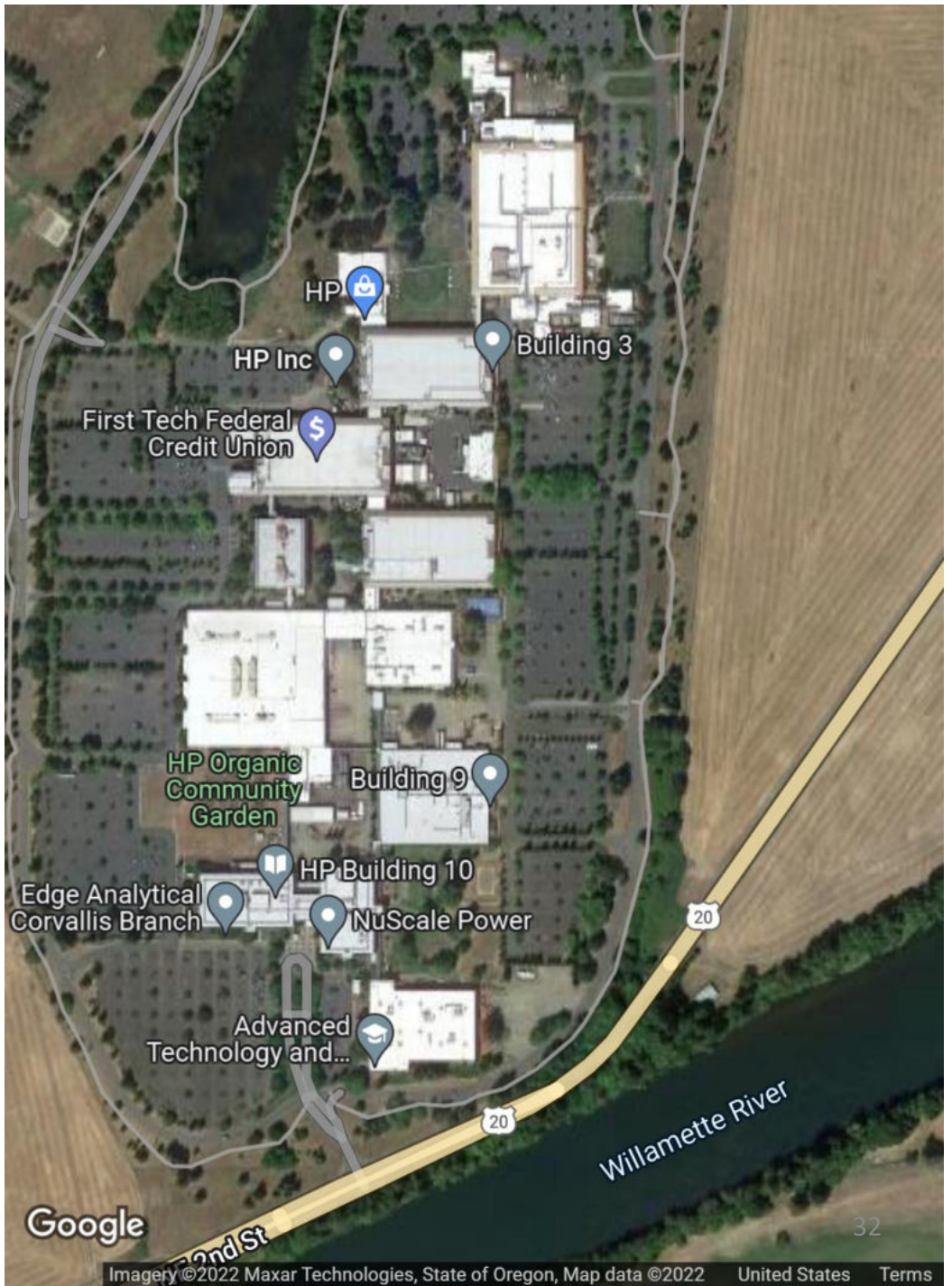
Even later

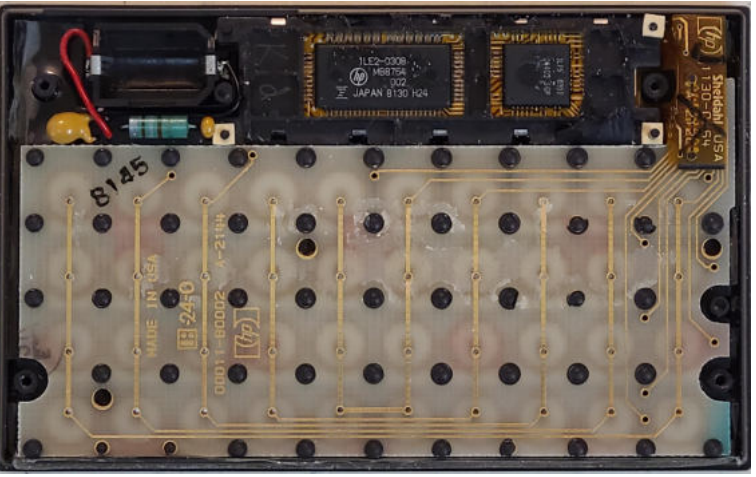
- Other buildings as IJBU grew

At one time before Compaq acquisition Corvallis site was HP's largest site

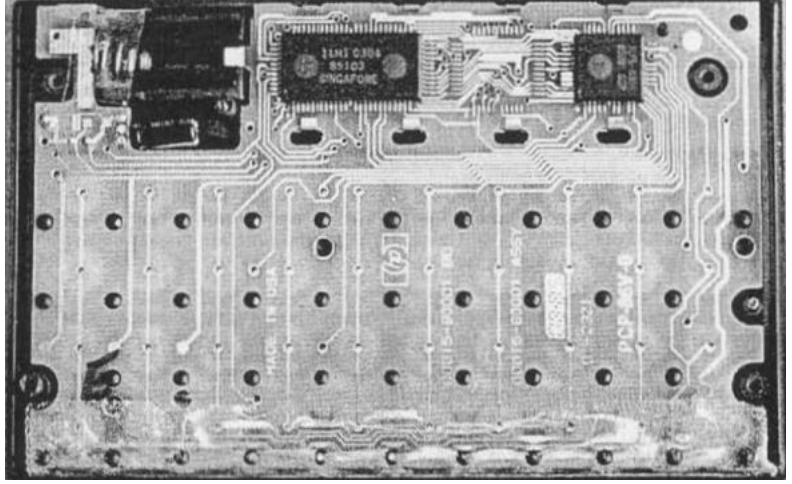
1010 NE Circle Blvd Site Today

- HP is still there, not occupying all the buildings
- Site is now a business park
- Demolished unused B1 office building

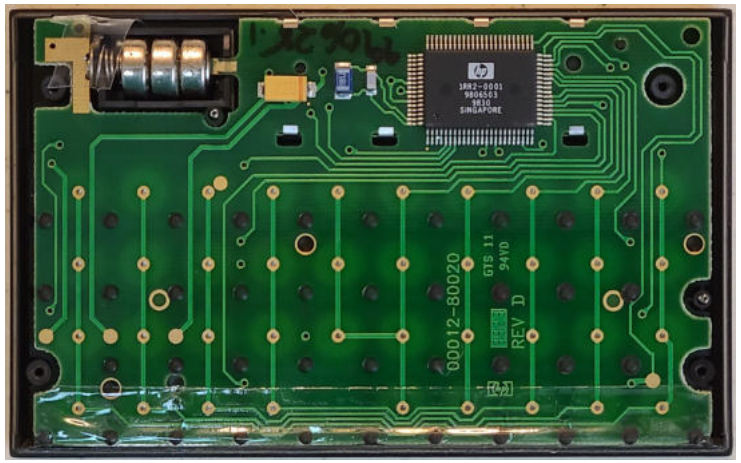




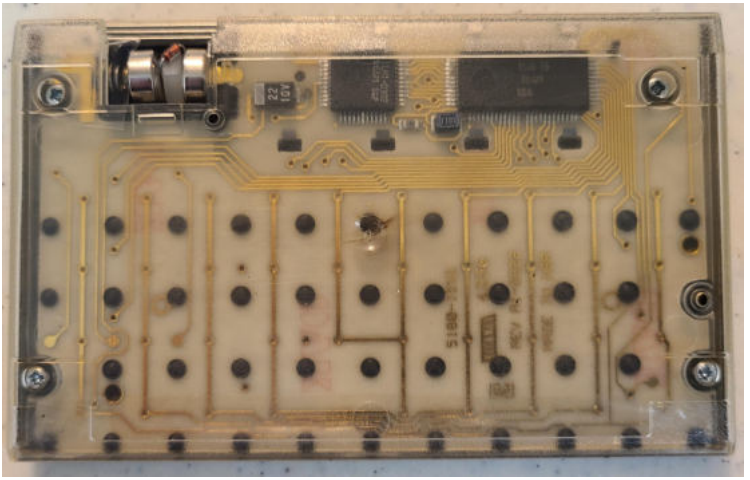
HP12C 1982wk18 USA 2218A04935



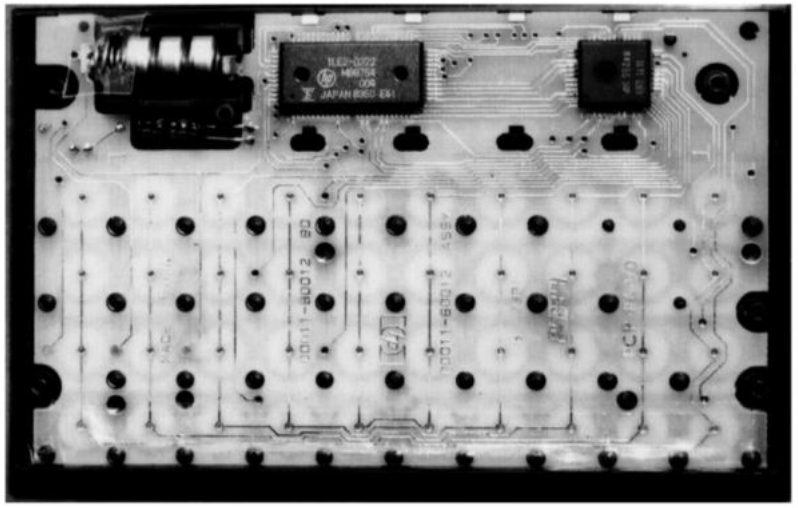
Post SST HP12



HP12C 1999wk29 Malaysia MY92902542



SST HP15



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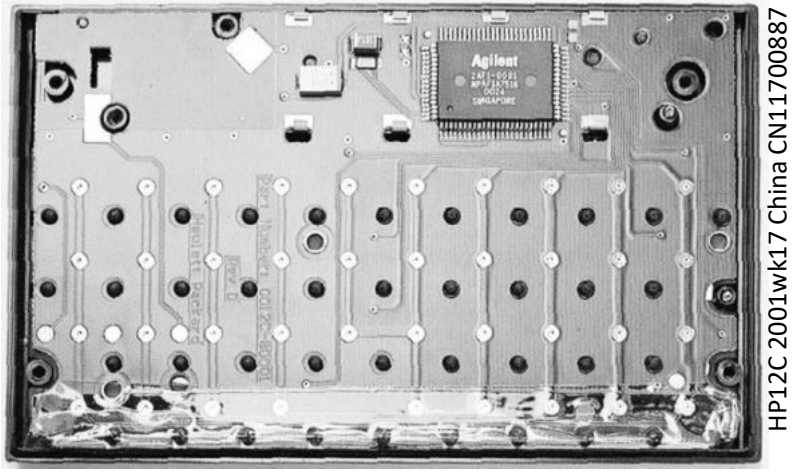

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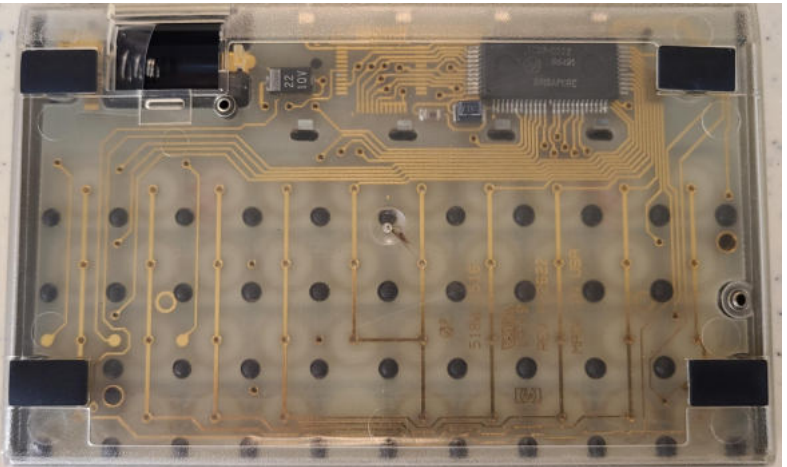
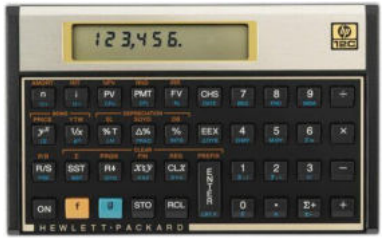


SST HP12 1982 USA 2222A#####

Voyager System



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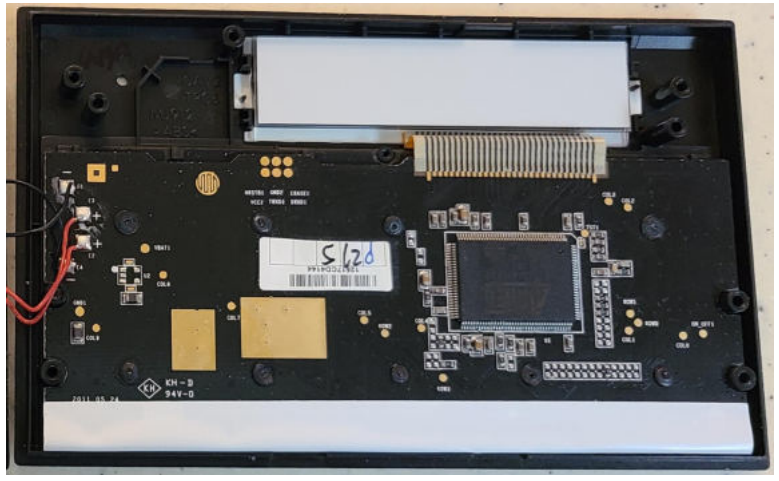
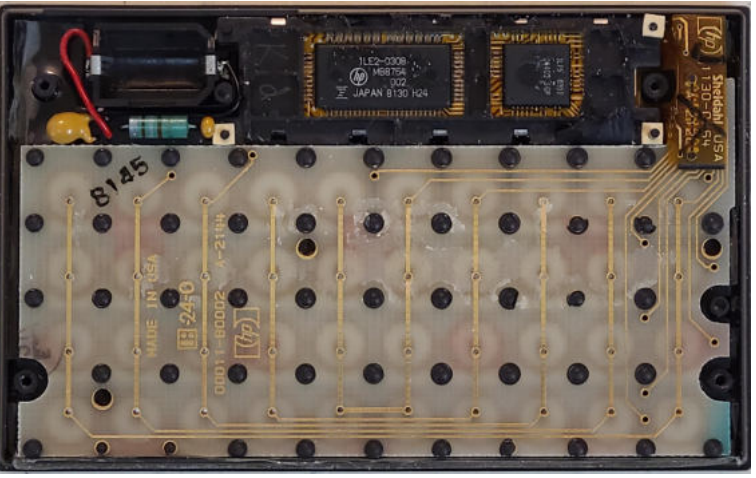


HP12C 2012 Invertec 4CY2320481



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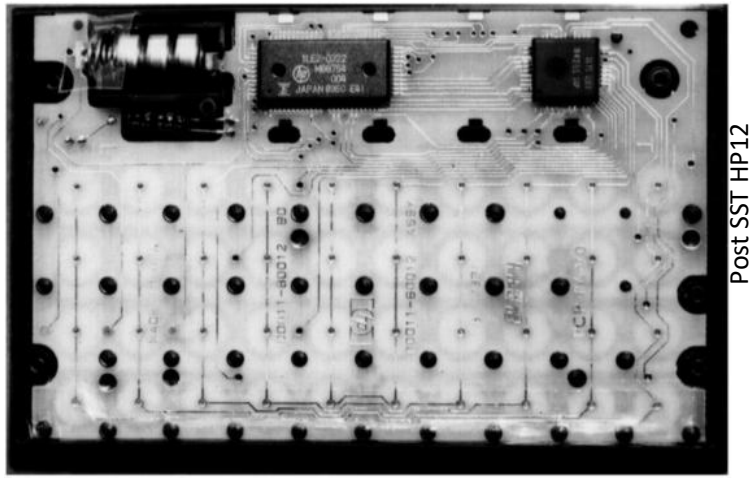
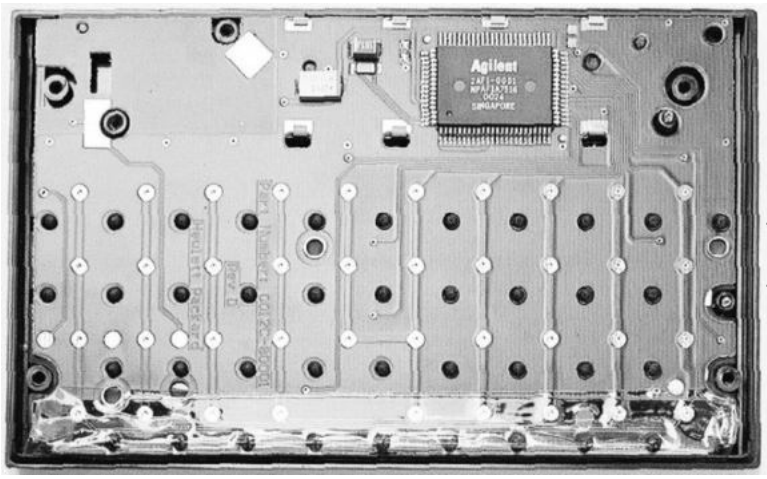


Post SST HP12



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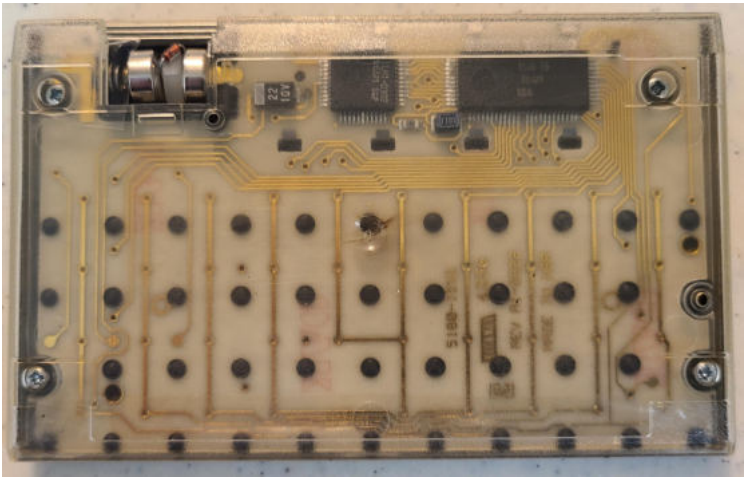
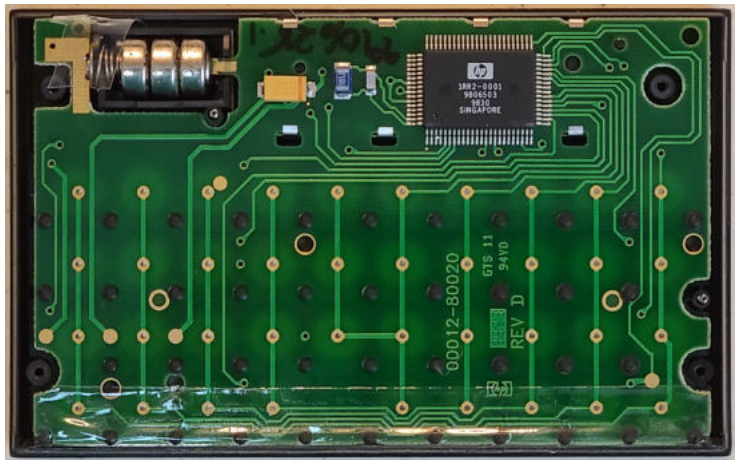


SST HP15



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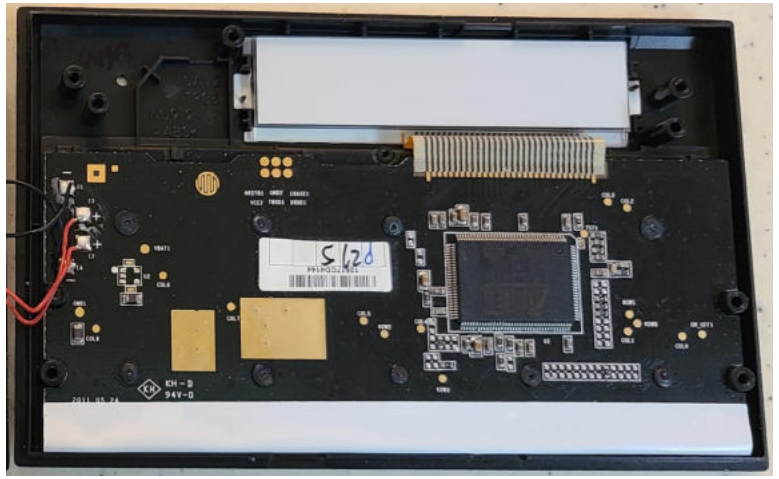

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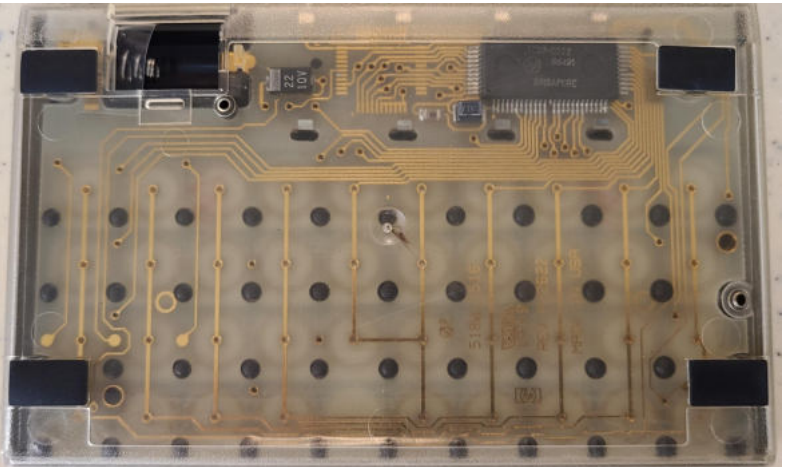

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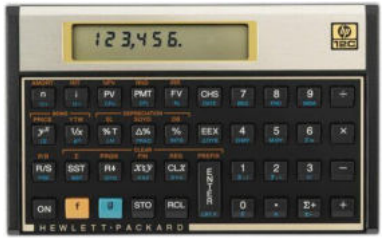

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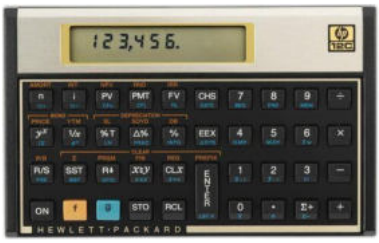

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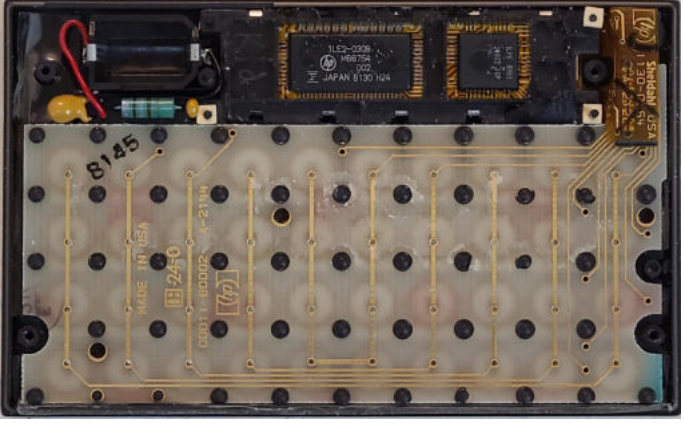

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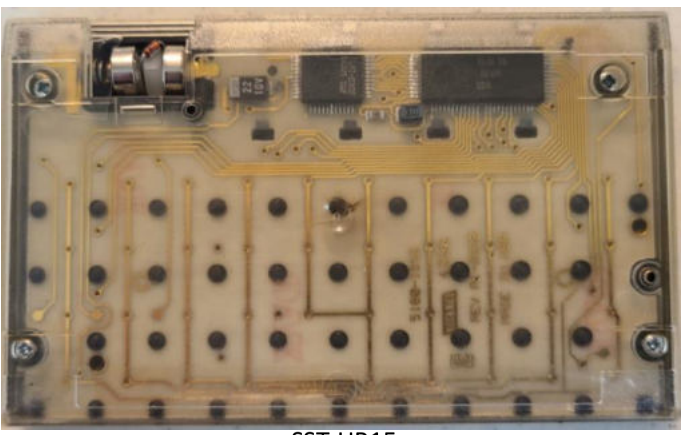
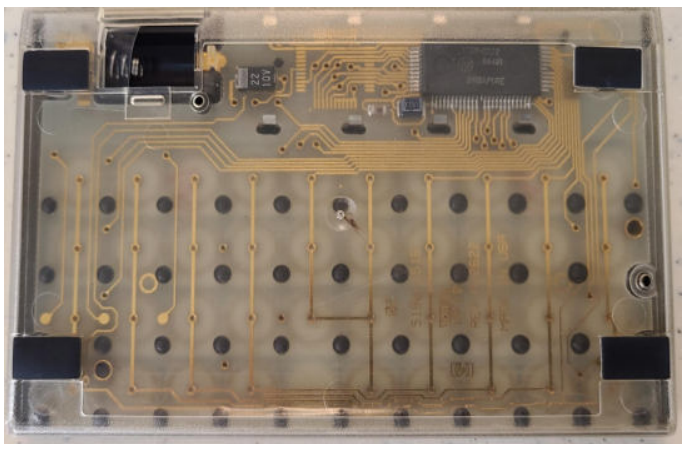


SST HP15



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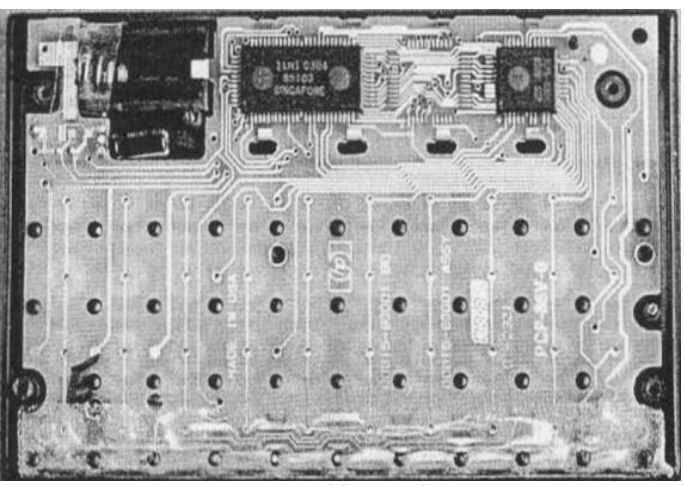

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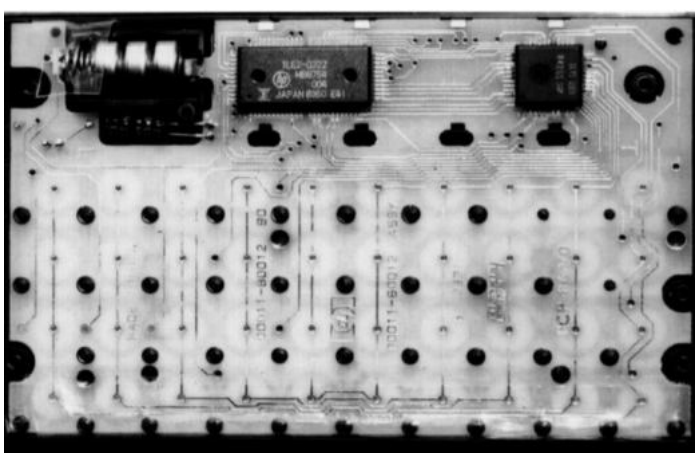

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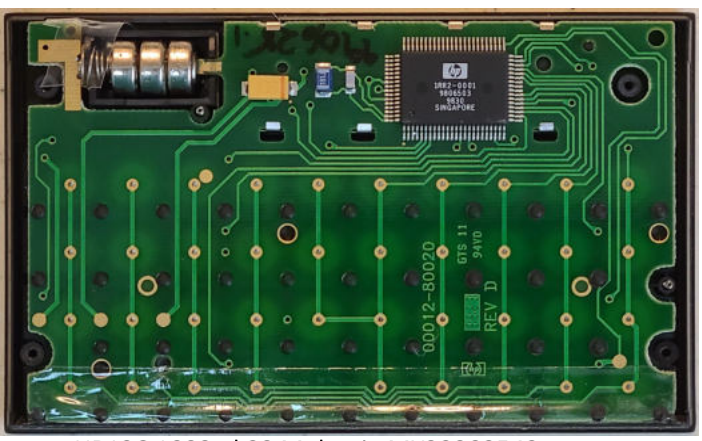

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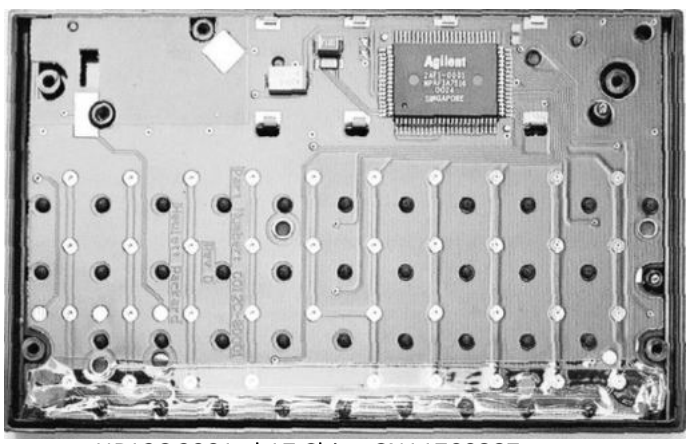

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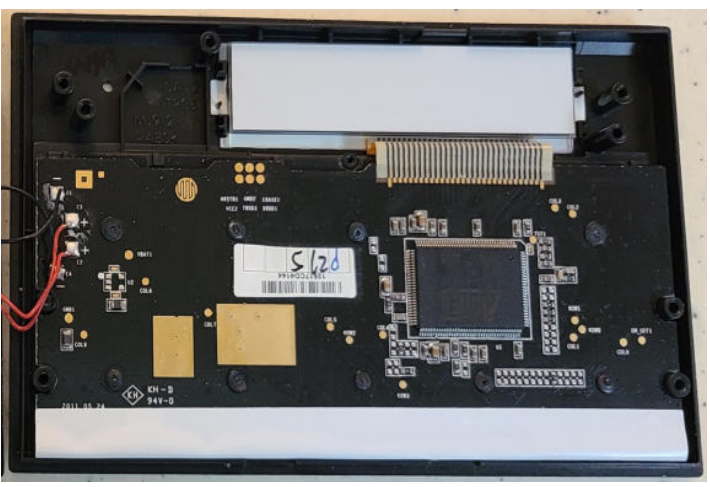

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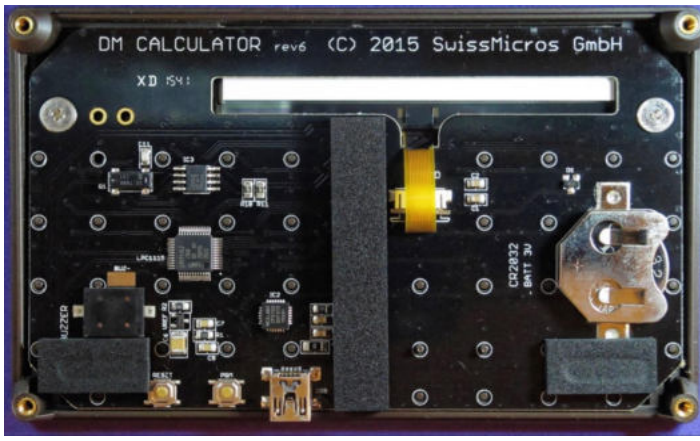

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