#### REPAIR OF A 1971 JAPANESE CALCULATOR CONTAINING UNDOCUMENTED JAPANESE MOS IC'S

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### The broken calculator : Riccar (TEAL fabrication, Tokyo 1971)



Japanese Calculator from 1971

Built by TEAL (Tokyo Electronic Applications Lab)

Resistor-Diode Logic Several undocumented Japanese MOS IC's (Mitsubishi & NEC; some hybrid blocks by Hitachi – display drivers )

From the era of the Calculator Wars https://www.youtube.com/watch?v=ansXGewduN4



### The broken calculator : Riccar (TEAL fabrication, Tokyo 1971)



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Tally memory (accumulate or substract using =+ or =-)

No technical documentation...

- Unknown architecture
- Unknown bit arithmetic
- Memory ?
- Registers and their size ?

#### The symptoms...



#### Internals



#### **Internals: double faced PCBs**



### **Unknown components**









#### Best way to communicate hidden or complex PCB tracks





# Electric design optimized for minimum components and cheap implementation of the logic



- Active devices (gain-providing) are PMOS transistors in ICs.
- Inverters, some gates, clocked flip-flops, and other more complex functions are provided in ICs.
- Most gates are constructed from discrete diodes and resistors in a variant of what may be called "Diode-AND-OR-Logic". Basic example shown to the left, note the opposing diode orientations.
- Numerous optimisations applied to reduce component count, tailored to individual circuits.
- The general DARL form originated earlier in the discrete days, used with bipolar transistors. Benefit was minimising the number of active devices needed, to keep costs down.
- DARL is not the same as DTL (Diode-Transistor-Logic).

# Electric design optimized for minimum components and cheap implementation of the logic



# Reverse engineering leading to a complete electrical schematic !

#### A few pages of the full schematic



2000 H-+





State Registers

Various Flags

Various Flags Addition/Substraction Logic

#### How the signals and their timing should look like...



#### Detailed understanding of the internal machine architecture...



# Distinguished 15 different states of the FSM and their function...

		State	Actions			
DEFAU	LT:		RX=>B	S=>RX	RY=>RY	RM=>RM
POC:	Power-On-Clear	0=>RM	0=>SNM	1=>OPAS,OPAM	KC	
KC:	Clear	0=>RX	0=>SND,SNO	0=>ERR	1=>OPAS,OPAM	? 0=>FKOP
ST11:	Idle loop, RX displayed.	FKOP-:S=>RY				
ST12:	Prepare RY for number entry. Clear DPD Counter. Clear Zero-Blanking Counter.	RX=>RX	0=>RY	0=>SND	0=>FDP	1=>ST12DONE
ST13:	Clear remnant digits in RX, shift PLC.(?)					
ST14:	Copy RM to RY. Olear Zero-Blanking Counter.	RM=>A	0=>B	FKOP-:S=>RY	SNM => SND	
ST15:	Add or Subtract to Memory Register. Clear Zero-Blanking Counter.			after		
ST21:	Shift RX down.		-C	P.N.		
ST22:	RY complemented into RX.	RY=>A	0=>B	B-A=1	SNO-=>SNO	
ST23:	Division: add back to correct overdraft.(?)	OPD:RY=>A				
ST24:	Primary arithmetic state for A,S,M & D. M: loop till D15=?. D: loop till Tens Carry @ ØD0.	RY=>A TC-:9=>A[14]	OPAS:A=>RY	enable B-A logic	PLC: 1=>FDAT	
ST25:	Shift RX up. OPM: shift PLC up. OPD: shift PLC up if FDP					
ST31:	Ø	OPE:1=>FKOP SND?SNO	DPa=>DPD RX shift?	FKOP-:DPD=>DF DPD shift?	Pa	
ST32:	Shift RY up till RY[12?] $\neq 0$ .	STRYLA: RX=>R	X, RY=>A, S=>RY	' 0=>PLC[14]		
ST33:	Clear RM if Recall.	FKOP-:RX=>RX 0=>FDAT-	FKOP-:RY=>A 0=>RX (•OPE)	FKOP-:S=>RY	0=>RM (•KT•KPF	3)
	Loop till KPN & KPR are released.		8 8			
ST34:	DP Alignment to Setpoint.	FKOP-:RX=>RX DPD no shift on	FKOP-:RY=>A ØD16	FKOP-:S=>RY	(RY clock alteratio	n)
	Shift DPD up until =ØDPS. Enter KNUM into bitstream (for KPN).					
ST35:	Idle loop for number entry, RY displayed.	0=>R[15] if no DP: DPD=0	FKOPNT:RX=>R ? SNO=0?	X,RY=>A,S=>RR2	0Mark=>PLO[14]	

Note: In multiplication and division, the Primary Loop is 24 -> 23 -> 25. The Secondary Loop is the self-loop on 24.

#### No instruction set All operations are hardwired



#### **Function of various undocumented Japanese IC's** deduced by logical reasoning



Function of new ones deduced by logical reasoning

#### **Confirmed by Japanese NEC databook, found later !**

### NEC エレクトロニクス データブック ELECTRONICS DATA BOOK '69

#### 日本電氣株式會計

#### 集積回路

µPB126D	•••••	(291)
$\mu PB127D$	•••••	(291)

アナログIC

105	
μPD 9 A	 (224)
μPD10A	 (227)
μPD11A	 (231)
µPD12A	 (235)
μPD13A	 (243)
$\mu PD14A\cdots$	 (246)
μPD15A	 (246)
μPD16A	 (249)
#PD101C	 (253)
#PD102C	 (253)
#PD103C	 (283)
µPD104C	 (283)
µPD105C	 (284)
µPD106C	 (284)
μPD107C	 (284)
µPD108C	 (285)
+PD109C	 (285)
#PD110C	 (286)
μPD111C	 (286)
#PD112C	 (286)
#PD116C	 (287)

µPC 1 A/1B ..... (164) "PC 3 A ..... (167) "PC 4 A ..... (171) "PC 6 A ..... (174) "PC7A/7B..... (178) "PC12B ..... (184) "PC16A/16C ..... (186)

#### #PC17C ...... (193) uPC23C ..... (294) "PC51A..... (197) uPC53A..... (197) µPC54C ..... (204) "PC55A ..... (206) <sup>1</sup>PC71A ..... (212) "PC91 C ...... (215) «PC92A ...... (218) uPC101B ..... (221) uPC103A ..... (292) #PC105A ..... (292)

#### 混成膜集積回路

MC-2527	 (257)
MC-2601	 (259)
MC-2602	 (259)
MC-2603	 (259)
MC-2621	 (260)
MC-2622	 (260)
MC-2623	 (260)
MC-2641	 (261)
MC-2642	 (261)
MC-2643	 (261)
MC-2675	 (266)
MC-4055	 (268)
MC-4056	 (269)
MC-4057	 (270)
MC-4058	 (271)
MC-4059	 (272)
MC-4075	 (273)
MC-4030	 (276)

#### **Confirmed by Japanese NEC databook, found later !**



#### Very big short circuit hampering repairs and tests



Quickly found by applying 2V, 1A and observing PCB with sensitive IR camera

After a few seconds: IC µPD105C broken...

Unavailable...

Needed a substitute... ?!?!

#### Peculiar supply voltages and switching behaviour of IC's

µPD13 MOSFET Transfer Curve

Vdd=-24V Rd=30K



Transition in  $V_d$  from 0 to -24V around  $V_q$  = -7V

No modern logic ICs have these characteristics, suitable discrete PMOS transistors were not readily found

Clever substitutes needed.





#### **Repairs needed of broken ring counter shift register IC**



One output (ΦD0) defective in M5812 6-bit ring counter shift register

Output regenerated using CD4013

Failed output at UK5.5.

Simple extension of shift register from ØD0-, clocked at end of digit by ØB8- +edge.

Zener reduces the JMOS supply voltage for the CMOS. Output transistor provides voltage isolation between CMOS and JMOS. Diode on inputs similarly provide voltage isolation.



# One inverter broken in two µPD13C IC's Substitute with PNP transistors



Replacement for failed MOSFET. Base current for bipolar should be acceptable here.

#### **Repairs needed of unavailable broken IC's**



More complex: 16 bit shift register Two alternatives with available CMOS IC's (but different voltage levels)



Careful implementation using PNP transistors at output and diode isolation at input!



PD105 Substitute Using 4517

#### **During repairs, with substitute on breadboard**



#### Final result: 6 faults repaired → working unit !



#### **Demonstration of working unit – powers of two !**



#### Puzzle: two ring registers → why ?



### **Undocumented feature discovered !**

Precision of constant of multiplication/division can be different from displayed decimal point

### Example:

Setting constant mode and 4 decimals after the comma: 5\*3.14159= 15.7295 (i.e. constant = 3.1415 – four decimal precision)

Setting now the display to 2 decimals after comma and repeating the calculation:

5= 15.72 i.e. calculation done to full precision of the constant and cut at 2 decimals

To compare: clearing the device and setting 2 decimals after the comma 5\*3.14= 15.70 i.e. entered decimals only to a precision of 2 after the comma

#### Conclusion: the constant multiplier can contain higher precision than the display...

#### Logic simulation of calculator

#### Translation of logic network in a sequence of "programme lines" Example:



#### Simulation programme shows details of operations

Operatio	on Sequence 💻		Registers		
flags	ofictator		Registers		
liags	UI States				
dns0 0PAS	AMA STIL	0 DPbort 0 SUB	3-0	R2- R3- SNahc-00	10
dps0 KPN~ . 0PAS~ 0PA	AM~ ST21~ PLC~=	0 DPb~=0. SUB	B=0 < -E B-> N=0 R1=	R2= R3= SNabc=00	10
dps0 KPN~ . OPAS~ OPA	AM~ ST12~ST13~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=0 R1=	R2= SNabc=00	0
dps0 KPN~ . OPAS~ OPA	AM~ ST21~ST35~ PLC~=	0 DPb~= SUB	3=0 <-E B-> N=1 R1=	R2= SNabc=00	0
dps0 KPN~ . OPAS~ OPA	AM~ ST15~ST34~ PLC~=	0 DPb~= SUB	B=1 <-E B-> N=0 R1=	R2= SNabc=00	10
dps0 KPN~ . UPAS~ UPA dps0	AM~ 5111~5133~ PLL~=	0 DPb~=	3=0 <-E B-> N=0 R1=	R2= SNabc=00 R2= R3= SNabc=00	10
dps0 0PAS~ 0PA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=0 R1=	R2=	0
dps0 0PAS~ 0PA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <−E B-> N=0 R1=	R2= SNabc=00	0
dps0 0PAS~ 0PA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <−E B-> N=0 R1=	R2= SNabc=00	10
KEYPRESS: KEY.4		0.005	0 N 0	D2 D2 CN-b - 00	
dos0 KPNa OPASa OPA	AM~ 5135~ PLL~=	0 DPb SUB	5=0 <-E B-> N=0 R1= B=0 <-E B-> N=0 P1=	R2=	10
dos0 KPN~ . OPAS~ OPA	AM~ ST35~ PLC~=		B=0 <-F B-> N=0 R1=	R2=	10
dps0 KPN~ . OPAS~ OPA	AM~ ST33~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=0 R1=	R2= SNabc=00	00
dps0 0PAS~ 0PA	AM~ ST33~ PLC~=	0 DPb~= SUB	3=0 <-E B-> N=0 R1=	R2= SNabc=00	0
dps0 0PAS~ 0PA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <−E B−> N=0 R1=	R2= SNabc=00	10
dps0 0PAS~ 0PA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=0 R1=	R2= SNabc=00	10
	AM~ 5135~ PLC~=	0 DPD~= SUB	3=0 <-E B-> N=0 KI=	R2= SNaDC≃00	10
dps0 OPAS~ OPA	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <−E B-> N=0 R1=	R2= SNabc=00	00
dps0 KPO~ . OPAS~ OPA	AM~ ST35~ PLC~=	0 DPb~=0 SUB	B=0 <-E B-> N=0 R1=	R2= SNabc=00	0
dps0 KPO~ . OPAS~ OPA	AM~ ST35~ PLC~=	0 DPb~=0 SUB	B=0 <-E B-> N=0 R1=	R2= SNabc=00	0
dps0 KPO~ . OPAS~ OPA	AM~ ST34~ PLC~=	0 DPb~=0 SUB	3=0 <-E B-> N=0 R1=	R2= SNabc=00	10
dps0 0PAS~ 0PA	AM~ ST34~ PLC~=	0 DPb~=0 SUB	3=0 <-E B-> N=0 R1=	R2= SNabc=00	0
dps0	AMA: ST15a: PLC~=	0 DPba- 0 SUB	S=0 <-E   D-> N=9 RI=4	R2=	10
dps0 0PAS~ 0PA	AM~ ST11~ PLC~=	0 DPb~=0 SUB	B=0 < -E B-> N=0 R1=4	R2=	0
dps0 0PAS~ 0PA	AM~ ST11~ PLC~=	0 DPb~=0 SUB	B=0 <-E B-> N=0 R1=4	R2= SNabc=00	0
dps0 0PMD~ 0PA	AM~ ST11~ PLC~=	0 DPb~=0 SUB	B=0 <−E B−> N=0 R1=4	R2= SNabc=00	0
KEYPRESS: KEY.5					
dps0 OPMD~ OPA	AM~ ST11~ PLC~=	0 DPb~=	B=0 < -E   B -> N=0 R1 =4	R2= SNabc=00	10
dos0 . KPN~ . OPMD~ OPA	AM~ ST11~ PLC~=		B=0 <-E B-> N=0 R1=4	R2=	10
dps0 KPN~ . OPMD~ OP/	AM~ ST35~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=1 R1=4	R2= SNabc=00	00
dps0 KPN~ . OPMD~ OPA	AM~ ST34~ PLC~=	0 DPb~= SUB	B=0 <−E B-> N=0 R1=4	R2= SNabc=00	10
dps0 KPN~ . OPMD~ OPA	AM~ ST33~ PLC~=	0 DPb~= SUB	B=0 <-E B-> N=0 R1=4	R2= SNabc=00	10
dps0 OPMD~ OPA	AM~ ST33~ PLC~=		$B=0 < -E   B -> N=0 R1 = \dots 4$	R2= SNabc=00	0
dps0 0PMD~ 0P/	AM~ 5135~ PLC~=	0 DPb SUB	$S=0 < -E   B -> N=0 RI= \dots 4$	RZ= SNaDC=00	10
dps0 OPMD~ OP/	AM~ ST35~ PLC~=	0 DPb~=	B=0 < -E B-> N=0 R1=4	R2=	10
KEYPRESS: KEY.6					1 <del>7</del> 11
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= SNabc=0	000
dps0 KPN~ . OPMD~ OP/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= 5 R3= SNabc=0	000
dps0 KPN~ . OPMD~ OP/	AM~ ST34~ PLC~=	0 DPb~= SU	B=0 < -E B-> N=0 R1=4	R2= SNabc=0	900
dps0 . KPN~ . UPMD~ UP/	AM~ 5133~ PLL~=	0 DBb-=	B=0 < E B > N=0 R1=4	KZ=	100
dos0 OPMD~ OP/	AM~ 5135~ PLC~=	0 DPb~=	B=0 < -E   B -> N=0   R1 =	R2=	100
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= 56 R3= SNabc=0	000
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= SNabc=0	000
KEYPRESS: KEY.7		n en			
dps0 OPMD~ OP/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E   B-> N=0 R1=4	R2= SNabc=0	000
dps0 . KPN~ . UPMD~ 0P/	AM- 5135~ PLC~=	0 DBP	B=0 < E B > N=1 RI=4	KZ=	000
$dps0$ , $KPN_{\sim}$ , $OPMD_{\sim}$ , $OP$	AM~ ST33~ PI (~=		B=0 <-F   B-> N=0 B1=	R2=	100
dps0 0PMD~ 0P/	AM~ ST33~ PLC~=	0 DPb~= SU	B=0 <-E   B-> N=0 R1=4	R2=	000
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E   B-> N=0 R1=4	R2= SNabc=0	000
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= SNabc=0	000
dps0 0PMD~ 0P/	AM~ ST35~ PLC~=	0 DPb~= SU	B=0 <-E B-> N=0 R1=4	R2= SNabc=0	100

#### **Simulation example**

4 \* 567 = 2268

	Operation	Seque	nce Primary			Re	egisters		
	flags	of sta	tes Loop Count	er		1	Ŭ		
	4	Ţ	J.						
KEYPRESS: KEY.=	•	•	V		25	<b>*</b>	<b>V</b>	<b>V</b>	
dps0	OPMD~ OPAM~	ST35~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	8 R1=4	R2=567	R3=	SNabc=000
dps0 KP0~ .	OPMD~ OPAM~	ST35~	PLC~=0	DPb~=0	SUB=0 < -E B-> N=0	0 R1 = 4	R2=	R3=	SNabc=000
dps0 KP0~ .	OPMD~ OPAM~	ST34~	PLC~=	DPb~=	SUB=0 <-E B-> N=0	R1=4	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST34~	PLC~=	DPb~=0	SUB=0 <-E B-> N=0	R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST32~	PLC~=0	DPb~=0	SUB=0 <-E B-> N=0	8 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST31~	PLC~=0	DPb~=0.	SUB=0 <-E   B-> N=0	8 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	5125~	PLC~=	DPD~=	SUB=0 <-E   B-> N=0	0 R1=4.	RZ=	R3=	SNabc=000
dos0	OPMD~ OPAM~	ST25~	PI C~=	DPb~=	SUB=0 <-E B-> N=0	R1=4.	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	8 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	5125~	PLC~=	DPb~=	SUB=0 < -E B-> N=0	0 R1=4	R2=	R3=	SNabc=000
dos0	OPMD~ OPAM~	ST25~	PLC~=	DPb~=	SUB=0 <-E   B-> N=0	R1=	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	0 R1=	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	5123~	PLC~=	DPD~=	SUB=0 <-E   B-> N=0	0 R1=4	R2=	R3=	SNabc=000
dns0		ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	R1=	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	5125~	PLC~=0	DPD~=	SUB=0 <-E   B-> N=0	0 R1=4	R2=	R3=	SNabc=000
dps0		ST25~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	R1=4	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST23~	PLC~=0	DPb~=	SUB=0 <-E B-> N=0	0 R1=4	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=.0	DPb~=	SUB=0 <-E   B-> N=0	0 R1=.4	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	5123~		DPb~=	SUB=0 <-E   B-> N=0	0 K1=.4	R2=	R3=	SNabc=000
dos0	OPMD~ OPAM~	ST23~	PI C~=0	DPb~=	SUB=0 <-E B-> N=0	R1=4	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST25~	PLC~=	DPb~=	SUB=0 <-E   B-> N=4	4 R1=	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST24~	PLC~=	DPb~=	SUB=0 <-E   B-> N=0	R1=567	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST24~	PLC~=0	DPb~=	SUB=0 <-E   B-> N=0	C R1=1134	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST24~	PLC~=0	DPb~=	SUB=0 <-E B-> N=E	B R1=17.1	R2=567	R3=	SNabc=000
dos0	OPMD~ OPAM~	5124~	PLC~=	DPD~=	SUB-0 <-E B-> N=/	A KI=	RZ=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST13~	PLC~=	DPb~=	SUB=0 <-EIB-> N=0	R1=	R2=	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST21~	PLC~=	DPb~=	SUB=0 <-E   B-> N=0	R1=2268	R2=	13=	SNabc=000
dps0	OPMD~ OPAM~	ST15~	PLC~=	DPb~=	SUB=0 <-E   B-> N=0	R1=	R2=567	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST11~	PLC~=0	DPb~=0	SUB=0 <-E B-> N=0	R1=	R2=2268	R3=	SNabc=000
dps0	OPMD~ OPAM~	ST11~	PLC~=0	DPD~=0	SUB=0 <-E  B-> N=0	R1=1	R2=	R3=	SNabc=000
COMMAND MODES	UPAS~ UPAM~	2111~	PLL~=0		208=0 <-F  R-> N=0	RI=	KZ=	NJE	SNapc=000
								Recht	

#### Simulation illustrating clever logic design

#### **Result of multiplication/division digitwise inserted in least significants digits of register !**

			Operation	Sequence	Primary	Decimal			RY	Tally Memory
			flags	of states	Loop Coun	ter Point		RX	(on Displa	v) (RM)
KEYPRESS:	KEY	.=		J.			6577		· .	
dps0		925	OPMD~ OPAM~	ST35- PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=	123 R2=	456 R3=\ SNabc=000
dps0	KP	0~ .	OPMD~ OPAM~	ST35~ PLC	~=0	DPb~=0	SUB=0 <-E   B->	N=0 R1=	123 R2=	
dps0	KP	0~ .	OPMD~ OPAM~	ST35~ PLC	~=0	DPb~=0	SUB=0 <-E   B->	N=0 R1=	123 R2=	456 R3= SNabc=000
dps0	KP	0~ .	OPMD~ OPAM~	ST34~ PLC	~=0	DPb~=0	SUB=0 <-E B->	N=0 R1=	123 R2=	456 R3= SNabc=000
dps0			OPMD~ OPAM~	ST34~ PLC	~=0	DPb~=0	SUB=0 <-E B->	N=0 R1=	123 R2=	456 R3= SNabc=000
dps0	10	20	OPMD~ OPAM~	ST32~ PLC	~=0	DPb~=0	SUB=0 <-E B->	N=0 R1=	123 R2=	456 R3= SNabc=000
dps0	- 12	204	OPMD~ OPAM~	ST31~ PLC	~=0	DPb~=0.	SUB=0 <-E B->	N=0 R1=	123 R2=	456 R3= SNabc=000
dps0		- C <b>P</b>	OPMD~ OPAM~	ST25~ PLC	~=0.	DPb~=0.	SUB=0 <-E B->	N=0 R1=	123. R2=	456 R3= SNabc=000
dps0			OPMD~ OPAM~	ST23~ PLC	~=0.	DPb~=	SUB=0 <-E B->	N=0 R1=	123. R2=	456 R3= SNabc=000
dps0			OPMD~ OPAM~	ST25~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 R1=	.123 R2=	/r/ pp =================================
dps0		105	OPMD~ OPAM~	ST23~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 R1=	.123 R2=	Multiplication timing =000
dps0	•	135	OPMD~ OPAM~	ST25~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 R1=	123 R2=	
dps0			OPMD~ OPAM~	ST23~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 R1=	123 R2=	=000
dps0	14		OPMD~ OPAM~	ST25~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=1	23 R2=	depends on =000
dps0		89 <b>4</b>	OPMD~ OPAM~	ST23~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=1	23 R2=	
dps0	•		OPMD~ OPAM~	ST25~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=12	3 R2=	
dps0	•	•	OPMD~ OPAM~	ST23~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=12	3 R2=	
dps0	•	•	OPMD~ OPAM~	ST25~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=123	R2=	=000
dps0	•	5. C	OPMD~ OPAM~	ST23~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=123	R2=	This case: $\sim 0.2s^{-1000}$
dps0	•	135	OPMD~ OPAM~	ST25~ PLC	~=	DPb~=	SUB=0 <-E B->	N=0 R1=123.	R2=	
dps0	•		OPMD~ OPAM~	ST23~ PLC	~=	DPD~=	SUB=0 <-E B->	N=0 R1=123.	R2=	
dps0		÷.	OPMD~ OPAM~	ST25~ PLC	~=	DPD~=	SUB=0 <-E B->	N=0 R1=123	RZ=	$(Maximum \sim 0.5S)$
dps0			OPMD~ OPAM~	ST25~ PLC	~=	DPD~=		N=0 R1=123	RZ=	-000
dps0		2.4	OPMD~ OPAM~	5125~ PLC	~=0	DPD~=	SUB=0 <-E B->	N=0 R1=123	RZ=	(54 P2- SNaba-999
dps0	•		OPMD~ OPAM~	ST25~ PLC		DPD~=		N=0 R1=123	R2	(54 P2- SNabo-000
dps0			OPMD~ OPAM~	ST22~ PLC	~=0	DPD~=		N=0 R1=123	R2=	(56 P2- SNabc-000
dps0	•	10	OPMD~ OPAM~	ST25~ PLC		DPb~=		N=0 R1=123	D2-	(56 P2- SNabc-000
dps0	•	135		ST23~ PLC	~= 0	DPb~=	SUB-0 <-E B->	N=0 R1=123	R2	456 P3= SNabc=000
dps0			OPMD~ OPAM~	ST25~ PLC	~= 0	DPb~=	SUB-0 C-E B->	N=0 R1=12	P2=	(56 R3= SNabc=000
dps0		003	OPMD~ OPAM~	ST23~ PLC	~= 0	DPb~=	SUB-0 C-E B->	$N=0$ $H_{1}= 123$	P2=	450 P3= SNabc=000
dps0		00	OPMD~ OPAM~	ST25~ PLC	~=0	DPb~=	SUB=0 <-E B->	=0 R1=123	R2=	456 R3
dps0		05	OPMD~ OPAM~	ST23~ PLC	~=0	DPb~=	SUB=0 <-E B	N=0 R1=123		456 R3=
dps0		- 5	OPMD~ OPAM~	ST25~ PLC	~=.0	DPb~=	SUB=0 <-E	N=1 R1=23		
dps0		10	OPMD~ OPAM~	ST24~ PLC	~=.0	DPb~=	SUB=0 <-F B->	N=A R1=23		
dps0		100	OPMD~ OPAM~	ST23~ PLC	~=.0	DPb~=	SUB=0 <	N=0 R1=23		
dps0		100	OPMD~ OPAM~	ST25~ PLC	~=0	DPb~=	SUB=0 < E B->	N=2 R1=3		
dps0			OPMD~ OPAM~	ST24~ PLC	~=0	DPb~=	SUB=0 < E B->	N=B R1=3		
dps0			OPMD~ OPAM~	ST24~ PLC	~=0	DPb~=	SUB=0 <- E B->	N=A R1=3		
dps0		87	OPMD~ OPAM~	ST23~ PLC	~=0	DPb~=	SUB=0 <  B->	N=0 R1=3		
dps0		92	OPMD~ OPAM~	ST25~ PLC	~=	DPb~=	SUB=0 <-E B->	N=3 R1=	.5472. R2=	
dps0			OPMD~ OPAM~	ST24~ PLC	~=	DPb~=	SUB=0 <-E b->	N=C R1=	.55176 R2=	
dps0			OPMD~ OPAM~	ST24~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=B R1=	.55632 R2=	
dps0			OPMD~ OPAM~	ST24~ PLC	~=0	DPb~=	SUB=0 <-E B->	N-1 R1=	.56.88 R2=	
dps0			OPMD~ OPAM~	ST23~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 H	56.88. R2=	/ 36 R3= SNabc=000
dps0			OPMD~ OPAM~	ST13~ PLC	~=0	DPb~=	SUB=0 <-E B->	N=0 R1=	56.88. R2=	456 R3= SNabc=000
dps0	$\sim$	194	OPMD~ OPAM~	ST21~ PLC	~=0	DPb~=	Desul		.50.00 KZ=	456 R3=. \abc=000
dps0	$\sim$	82	OPMD~ OPAM~	ST15~ PLC	~=0	DPb~=	Kesul	. III Кλ	.56.88 R2=	456 R3=. Copied in RY Vabc=000
dps0.			OPMD~ OPAM~	ST11~		DPb~=0	(123 * 156	5 = 56088)	.56.88 R2=	56.88 R3=. \abc=000
dps0			OPMD~ OPAM~	ST11~ Decim	nal Point Set	DPb~=0	(120 400		.56.88 R2=	56.88 R3=. TOT CISPIAY Vabc=000
dps0	•	0.	OPAS~ OPAM~	ST11~	0	DPb~=0	SUB=0 <-E B->	N=0 R1=	.56.88 R2=	56.88 R3=

## In progress: simulation with Digital logic software (H.Neemann)

Digital input files are ready and being tested Possibly an issue with propagation delays

Under discussion with the author of Digital (H.Neemann)

Hope to find a solution...

Suggestions for other logic software packages ?

#### Successful repair of a 1971 Japanese calculator... over the internet !!

#### Unique, very instructive and extremely pleasant experience Discussing and exchanging information ~ 10000km away by internet ...

- No documentation on calculator, function of several IC's unknown at start...
  - Function of IC's derived by logic reasoning by B.Hilpert; confirmed by Japanese databooks, found later
  - Full reverse engineering of the PCBs by B.Hilpert, exchanging detailed photos / pptx for hidden tracks
- Technical advice and insights in logic by B.Hilpert
- Six major faults found and repaired
  - Substitutes for unavailable IC's carefully designed by B.Hilpert
  - Broken track (?) / bad contact (?) found
- Simulation program by B.Hilpert: very instructive to understand logic design 
   full and detailed understanding of design and implementation
- Undocumented features discovered
- In progress: simulation with logic software "Digital" / Discussion with H.Neemann More info on this project (and many other interesting subjects): http://madrona.ca

### HOPE YOU ENJOYED THE PRESENTATION

### THANK YOU FOR YOUR ATTENTION